ETM19E-02

EPSON TOYOCOM

Application Manual

Real Time Clock Module

RX-4575LC

EPSON TOYOCOM CORPORATION

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CONTENTS

Small-Sized Real Time Clock Module with Event Detecting Function

RX – 4575 LC

- Interface system : 3-wire serial interface
- Interface voltage range : 1.6 V ~ 5.5 V
- Clock (holding) voltage range : 1.3 V ~ 5.5 V
- Backup electricity consumption : 0.32 μA / 3 V (Typ.)

External event detecting function : In addition to chattering absorbing rate, it is able to set positive logic and negative logic.

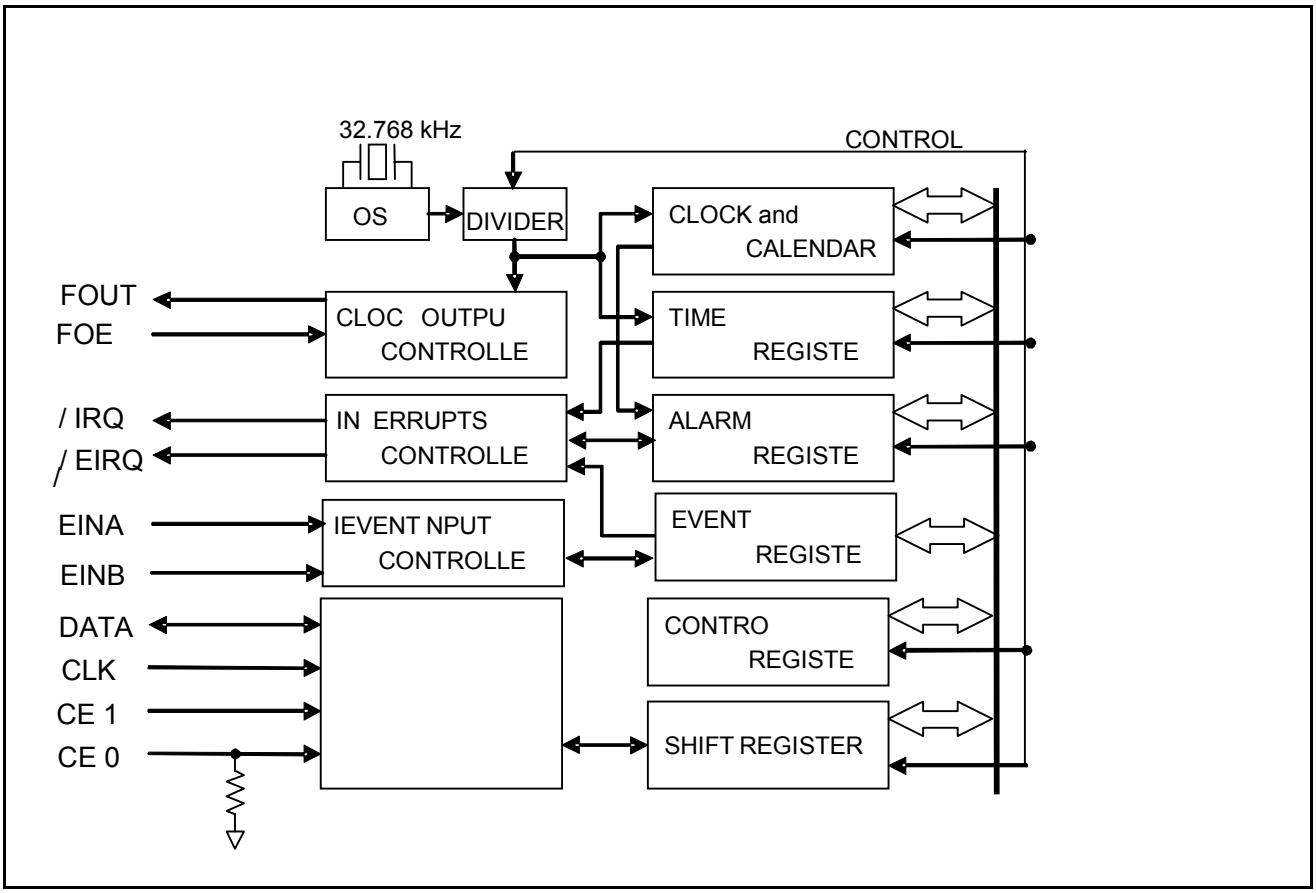
- 32.768 kHz output function : C-MOS output with output control function
- Real time clock function

  Clock / Various interrupt functions such as full auto calendar, alarm, timer, external input detection etc.

1. Overview

This is a serial interface system real time clock RTC with a built-in precision crystal unit with 32.768kHz. Equipped with 2 chattering-free signal input port, which is able to detect various event such as switch input, interrupt signal etc. correctly to implement interrupt information to CPU. Further, it has various functions such as alarm, timer interrupt built-in based on auto-calendar clock function so that it makes great contribution to optimization and increasing efficiency to distribute system resource.
Device is designed taking low current consumption into consideration based on C-MOS process, and therefore it is the most suitable to apply to small-sized electronic equipment such as DSC, PDA, handy-terminal etc. which are required long period battery backup.

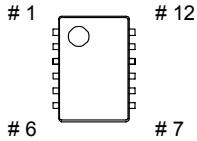
2. Block Diagram



3. Terminal Discription

3.1. Terminal Connections

RX-4575LC



VSOJ - 12pin

3.2. Pin Function

Signal Name	Input/ Output	Functions
CE0	Input	Chip enabled 0 input pin with built-in pull-down resistors. When both CE0 and CE1 pins are at the "H" level, accessable to the RTC.
CE1	Input	This is a chip enabled 1 input pin. When both CE0 and CE1 pins are at the "H" level, accessable to the RTC.
CLK	Input	Shift clock input pin for serial data transfer. During write mode, takes data from DATA pin with CLK signal rising edge, and output data from DATA pin with falling edge during read mode.
DATA	Bi-directional	Data input/output pin for serial data transfer. By setting of mode after input of CE0 or CE1 rising, it is able to apply to input or output pin.
EINA	Input	It is able to detect input of logic signal. It is able to select Hi detection, Low detection, pullup resistance option and pulldown option by means of register setting. When detect input, it is able to output interrupt signal.
EINB	Input	It is able to detect input of logic signal. It is able to select Hi detection, Low detection, pullup resistance option and pulldown option by means of register setting. When detect input, it is able to output interrupt signal.
FOUT	Output	Output pin with 32.768kHz with output control function by FOE input pin and FE bit. With C-MOS output, it is high impedance condition in case output is off,.
FOE	Input	If one of FOE pin or FE bit is “H”, 32.768kHz is output from FOUTpin. If both FOE pin and FE bit are “L”, FOUT pin is in high impedance condition.
/ EIRQ	Output	Open drain output pin for event detecting interrupt. It is also able to output alarm and interrupt timer.
/ IRQ	Output	Open drain output pin for alarm and timer interrupt.
VDD	–	Connect to the plus side of power.
GND	–	Copnnect to the ground.

Note : Be sure to connect a bypass capacitor rated at least 0.1 µF between VDD and GND.

4. Absolute Maximum Ratings

GND = 0V

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	–	–0.3 ~ +7.0	V
Input voltage	V_{IN}	Input pin	GND–0.3 ~ V_{DD}+0.3	V
Output voltage (1)	V_{OUT1}	Pullup voltage of / IRQ, / EIRQ pin	GND–0.3 ~ +8.0	V
Output voltage (2)	V_{OUT2}	FOUT, DATA	GND–0.3 ~ V_{DD}+0.3	V
Storage temperature	T_{STG}	Separated storage without packing	–55 ~ +125	°C

5. Recommended Operating Conditions

GND = 0V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{DD}	–	1.6	3.0	5.5	V
Clock supply voltage	V_{CLK}	–	1.3	3.0	5.5	V
Operating temperature	T_{OPR}	No condensation	–40	+25	+85	°C

6. FrequencyCharacteristics

GND = 0V

Item	Symbol	Condition	Rating	Unit
Frequency precision	$\Delta f / f$	Ta = +25 °C, V_{DD} = 3.0 V	5 ± 23 (*1) (*2)	$\times 10^{-6}$
Frequency/voltage characteristics	f / V	Ta = +25 °C, V_{DD} = 2.0 V ~ 5.0 V	± 2 Typ.	$\times 10^{-6}$ / V
Frequency/temperature characteristics	Top	Ta = –20 °C ~ +70 °C, V_{DD} = 3.0 V ; +25 °C reference	+10 / –120	$\times 10^{-6}$
Oscillation start time	tSTA	Ta = +25 °C, V_{DD} = 1.6 V	1 Max.	s
		Ta = – 40 °C ~ +85 °C V_{DD} = 1.6 V	3 Max.	s
Aging	fa	Ta = +25 °C, V_{DD} = 3.0 V ; firast year	± 5 Max.	$\times 10^{-6}$ / year

*1) This difference is 1 minute by 1 month. (excluding offset)

*2) Including the frequency variation arising from two reflow processing's
*: Reflow processing as conducted under Epson's conditions (Refer to the individual l specification).

7. Electrical Characteristics

7.1. DC characteristics

* Unless otherwise specified, GND = 0 V , V_{DD} = 1.6 V to 5.5 V , Ta = –40 °C to +85 °C

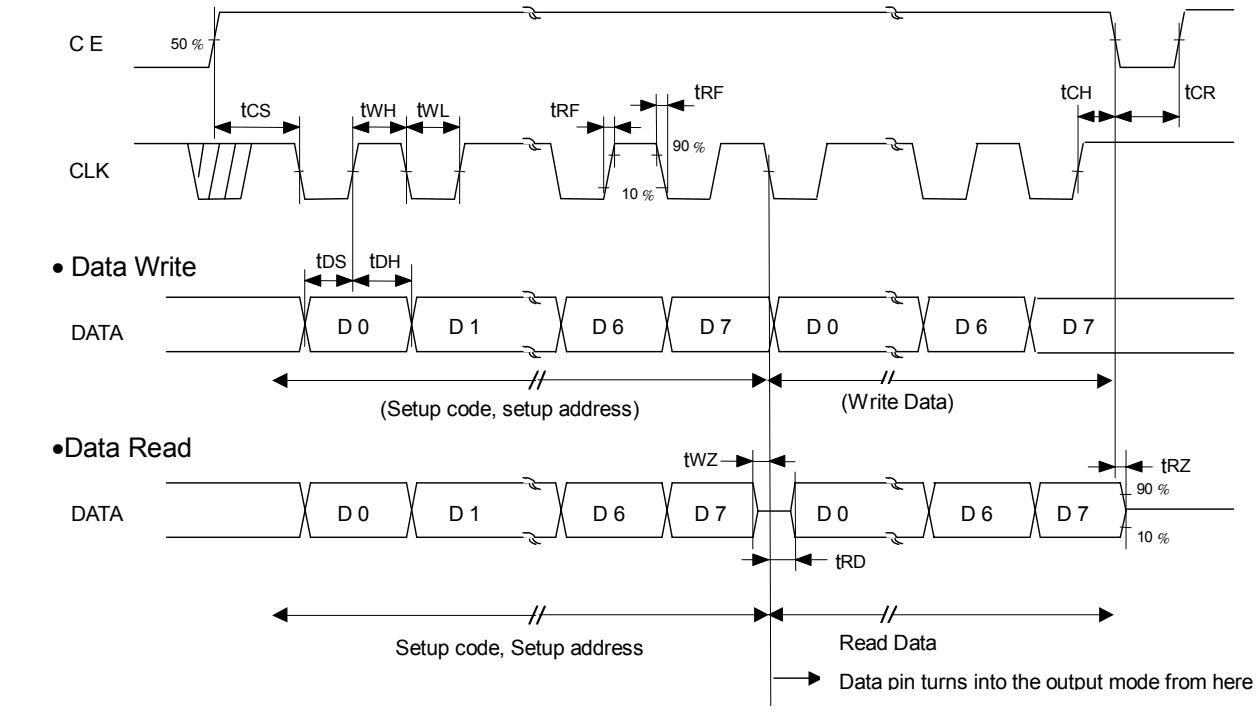
Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption (1)	I_{DD1}	CE0,CE1,CLK,EINA,EINB,FOE=VSS DATA,IRQ,EIRQ=VDD FOUT Output OFF(Hi-Z) Event detection OFF REA,REB,EA,EB bit= "0"	V_{DD} = 5 V		0.45	(0.9)	µA
Current consumption (2)	I_{DD2}		V_{DD} = 3 V		0.32	(0.7)	
Current consumption (3)	I_{DD3}	CE0,CE1,CLK,EINA,EINB=VSS FOE,DATA,IRQ,EIRQ=VDD FOUT Output ON(32.768kHz),CL=0pF Event detection 7.8ms operation REA,REB bit= "0" HLA,HLB,EA,EB,T0,T1 bit= "1"	V_{DD} = 5 V		3.0	(7.5)	µA
Current consumption (4)	I_{DD4}		V_{DD} = 3 V		1.7	(4.5)	
Current consumption (5)	I_{DD5}	CE0,CE1,CLK,EINA,EINB=VSS FOE,DATA,IRQ,EIRQ=VDD FOUT Output ON(32.768kHz),CL=30pF Event detection 7.8ms operation REA,REB bit= "0" HLA,HLB,EA,EB,T0,T1 bit= "1"	V_{DD} = 5 V		8.0	(20.0)	µA
Current consumption (6)	I_{DD6}		V_{DD} = 3 V		5.0	(12.0)	
High-level input voltage	V_{IH1}	CE0, CE1, CLK, DATA, FOE EINA, EINB pins		0.7 × V_{DD}		V_{DD} + 0.3	V
	V_{IH2}	Pullup voltage of / EIRQ, / IRQ pins				6.0	V
Low-level input voltage	V_{IL}	CE0, CE1, CLK, DATA, FOE EINA, EINB pins		GND – 0.3		0.3 × V_{DD}	V
High-level output voltage	V_{OH1}	DATA, FOUT pins	V_{DD} = 5 V, I_{OH} = –1 mA	4.5		5.0	V
	V_{OH2}		V_{DD} = 3 V, I_{OH} = –1 mA	2.2		3.0	
	V_{OH3}		V_{DD} = 3 V, I_{OH} = –100 µA	2.9		3.0	
Low-level output voltage	V_{OL1}	DATA, FOUT pins	V_{DD} = 5 V, I_{OL} = 1 mA	GND		GND+0.5	V
	V_{OL2}		V_{DD} = 3 V, I_{OL} = 1 mA	GND		GND+0.8	
	V_{OL3}		V_{DD} = 3 V, I_{OL} = 100 µA	GND		GND+0.1	
	V_{OL4}	/ EIRQ and / IRQ pins	V_{DD} = 5 V, I_{OL} = 1 mA	GND		GND+0.25	V
	V_{OL5}		V_{DD} = 3 V, I_{OL} = 1 mA	GND		GND+0.4	
Input resistance (1)	R_{DWN1}	CE0 pin	VDD=5V	75	150	300	kΩ
Input resistance (2)	R_{DWN2}	VIN=VDD	VDD=3V	150	300	600	kΩ
Input resistance (3)	R_{DWN3}	EINA,EINB pins	VDD=5V	15	30	60	kΩ
Input resistance (4)	R_{DWN4}	VIN=VDD	VDD=3V	30	60	120	kΩ
Input resistance (5)	R_{UP1}	EINA、EINB pins	VDD=5V	15	30	60	kΩ
Input resistance (6)	R_{UP2}	VIN=VSS	VDD=3V	30	60	120	kΩ
Input leakage current	I_{LK}	CE0 pin ; V_{IN} = GND CE1, CLK, FOE, EINA, EINB pins ; V_{IN} = V_{DD} or GND Built-in resistance OFF		–0.5		0.5	µA
Output leakage current	I_{OZ}	DATA, / EIRQ, / IRQ, FOUT oins, V_{OUT} = V_{DD} or GND		–0.5		0.5	µA

7.2 AC characteristics

* Unless otherwise specified, GND = 0 V , Ta = –40 °C to +85 °C

Item	Symbol	Condition	V_{DD} = 3 V ± 10 %			V_{DD} = 5 V ± 10 %			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
CLK clock cycle	t_{CLK}		600			350			ns
CLK H pulse width	t_{WH}		300			175			ns
CLK L pulse width	t_{WL}		300			175			ns
CE setup time	t_{CS}		300			175			ns
CE hold time	t_{CH}		300			175			ns
CE recovery time	t_{CR}		400			300			ns
Write data setup time	t_{DS}		75			50			ns
Write data hold time	t_{DH}		75			50			ns
Write data disable time	t_{WZ}		0			0			ns
Read data delay time	t_{RD}	CL = 50 pF			300			120	ns
Output disable time	t_{RZ}	CL = 50 pF RL = 10 kΩ			200			100	ns
Input rise/fall time	t_{RF}				100			50	ns
FOUT duty (when output at 32.768 kHz)	t_W / t	50 % V_{DD} Level	45		55	45		55	%

Timing chart



8. Overview of Functions and Description of Registers

8.1 Overview of Functions

1) Clock functions

This function is used to set and read out month, day, hour, date, minute, second, and year (last two digits) data. Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2099.

∗ For details, see "9.1. Description of Registers".

2) Fixed-cycle interrupts generation function

The fixed-cycle timer interrupt generation function generates an interrupt event periodically at any fixed cycle set between 244.14 μs and 4095 minutes.
When an interrupt event is generated, in addtion to interrupt hardware with LOW driving of the /IRQ pin, it is also able to detect software detection by read out judgment of timer flag bit.
This function can be selected from two types of operations (single-shot operations and repeated operations).

∗ For details, see "9.2. Fixed-cycle Interrupt Function". .

3) Alarm interrupt function

The alarm interrupt generation function generates interrupt events for alarm settings such as date, hour, and minute settings.
When an interrupt event is generated, in addtion to interrupt hardware with LOW driving of the /IRQ pin, it is also able to detect software detection by read out judgment of timer flag bit.

∗ For details, see "9.3. Fixed-cycle Interrupt Function". .

4) Clock output function

A clock with the same frequency (32.768 kHz) as the built-in crystal resonator can be output from the FOUT pin (CMOS output).
It is also possible to control output with both hardware and software in combination with FOEpin and FE bit.

5) Event detecting function

By having 2 logic input pins from outside, it is able to detect each event input.
When detect event, it is able to detect software by read out judgment of each event flag bit in addition to hardware interrupt with LOW driving of the/ ERQ pin.
Each event input pin is able to select optionally pullup and pulldown resistance individually, and is possible to do selecting set positive logic and negative logic respectively.

It is able to set filtering time of chattering from approx. 7.8ms to 125ms by reguster setting.
After detecting event, control input through current and detection operation current to continue internal pulldown resistance immediately and stop detection operation automatically.
Input condition of each event input pin is able to get software monitoring in a real-time through register bit.

∗ For details, see [9.4. Event detecting function] .

8.2. Register Table

Address	Functions	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Remarks
0	SEC	fos	40	20	10	8	4	2	1	
1	MIN	fr	40	20	10	8	4	2	1	
2	HOUR	fr	•	20	10	8	4	2	1	
3	Interrupt Setup	fr	MIE	SB	SA	AOF	TOF	AQ	TQ	
4	DAY	fr	•	20	10	8	4	2	1	
5	MONTH	fr	•	•	10	8	4	2	1	
6	YEAR	80	40	20	10	8	4	2	1	
7	MIN Alarm	AE	40	20	10	8	4	2	1	
8	HOUR Alarm	AE	•	20	10	8	4	2	1	
9	DAY Alarm	AE	•	20	10	8	4	2	1	
A	Input setup	T1	T0	HLB	HLA	UDB	REB	UDA	REA	
B	Event Detection	EIE	EB	EA	•	•	•	FB	FA	
C	Timer Setup	TE	FE	TD1	TD0	2048	1024	512	256	
D	Timer Counter	128	64	32	16	8	4	2	1	
E	Control Register 1	•	•	•	TI / TP	AF	TF	AIE	TIE	
F	Control Register 2	•	TEST	0	RESET	HOLD	•	•	•	

Not When after the initial power-up or when the result of read out the fos bit is "1" , initialize all registers, before using the module.
Be sure to avoid entering incorrect date and time data, as clock operations are not guaranteed when the data or time data is incorrect.

*1. When input initial power from 0(V, fos, REA, REB bit is set to “1”and each bit of EIE, AIE, TIE, MIE, TE, FE, TEST, EA, EB, UDA, UDB is cleared to “0”.

*2. The TEST bit is for our test purpose. Bit 5 t when writing.
Bit 5 of register F is always “0” and writing is unavailable.

*3. Bit with ”• ”mark can use as general purpose memory bit, we recommend you to fix to “0” in clock register or to give “0” mask after reading to avoid mismatching of the read values.

9. Description of Functions

9.1. Descriptipon of registers

9.1.1. Clock counter (Reg - 0[h] ~ 2[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	SEC	fos	40	20	10	8	4	2	1
1	MIN	fr	40	20	10	8	4	2	1
2	HOUR	fr	•	20	10	8	4	2	1

- **Counts [seconds], [minutes] and [hours].**
- The data format is BCD format. For example, when the "seconds" register value is "0101 1001" it indicates 59 seconds.
- The fr bit is flag bit that indicates the operation status of the RTC's internal clock counter.

∗ Note with caution that writing non-existent time data may interfere with normal operation of the clock counter.

1) [SEC] Register
This counter counts seconds.
Count values are updated in order 00 seconds, 01 second, 02 to 59 seconds, 00 seconds, 01 second, etc.

2) [MIN] Register
This counter counts minutes.
Count values are updated in order 00 minutes, 01 minute, 02 to 59 minutes, 00 minutes, 01 minute, etc.

3) [HOUR] Register
Counter that counts [hours] with the round-the-clock system.
Count values are updated in order 00 hours, 01 hour, 02 to 23 hours, 00 hours, 01 hour, etc.

4) fos bit (OSC Flag)
This is a flag bit that retains the result when this RTC's internal oscillation status is detected.
If the RTC's internal oscillation is stopped, such as when a drop occurs in the power supply voltage, the value of this bit changes from "0" to "1 ".
If this bit's value is "1" when read, this RTC's data is ignored, in which case all registers should be initialized before being used.

∗ This bit is set (= 1) during the initial power-on.
∗ After confirming that this bit's value is "1" when read, be sure to clear this fos bit to zero in preparation for the next detection operation.

5) fr bit (READ Flag)
This is a read-only flag bit that indicates the clock status when read.
If the clock counter is incremented during a read operation, the value of this bit changes from "0" to "1 ".
If this bit's value is "1" when read, it may be due to updating of other clock data, in which case all clock registers should be read again.

∗ This fr bit is automatically cleared to zero when the CE0 input pin or CE1 input pin goes to low level.
∗ The fr bits in Reg – 1 to 5 all have the same function.

9.1.3. Calendar counter (Reg - 04[h] ~ 06[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
4	DAY	fr	•	20	10	8	4	2	1
5	MONTH	fr	•	•	10	8	4	2	1
6	YEAR	80	40	20	10	8	4	2	1

- The auto calendar function updates all dates, months, and years from January 1, 2001 to December 31, 2099.
- The data format is BCD format. For example, a date register value of "0011 0001" indicates the 31st.

∗ Note with caution that writing non-existent date data may interfere with normal operation of the calendar counter.

1) [DAY] counter

- This is the date counter.
  Updating condition of this counter varies depending on the month.

∗ A leap year is set whenever the year value is a multiple of four (such as 04, 08, 12, 88, 92, or 96). In February of a leap year, the counter counts dates from "01," "02," "03," to "28," "29," "Mar. 01," etc.

DAY	Month	Date update pattern
Write/Read	1, 3, 5, 7, 8, 10, or 12	01, 02, 03 ~ 30, 31, 01 ~
	4, 6, 9, or 11	01, 02, 03 ~ 30, 01, 02 ~
	February in normal year	01, 02, 03 ~ 28, 01, 02 ~
	February in leap year	01, 02, 03 ~ 28, 29, 01 ~

2) [MONTH] counter

- This is the month counter.
  It is updated in order Jan. Feb. Mar. ~ Dec.Jan. Feb. etc.

3) [YEAR] counter

- This is the year counter.
  It is updated in order 00, 01, 02 ~ 99, 00, 01 etc.
- Any year that is a multiple of four (04, 08, 12, 88, 92, 96, etc.) is handled as a leap year.

9.1.4. Alarm register (Reg - 7[h] ~ 9[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
7	MIN Alarm	AE	40	20	10	8	4	2	1
8	HOUR Alarm	AE	•	20	10	8	4	2	1
9	DAY Alarm	AE	•	20	10	8	4	2	1

- The AIE bit and AFT bit can both be set or used when using alarm interrupt function to set interrupt events for dates, hours, minutes, etc.
- When the current time matches the settings in the above alarm registers, the AF bit's value is "1" and the AIRQ pin's status is low so that an alarm can be noticed with software or hardware.

* For details, see "9.3. Alarm Interrupt Function".

9.1.5. Event detection conuter (Reg - A[h] ~ B[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
A	Input setup	T1	T0	HLB	HLA	UDB	REB	UDA	REA
B	Event Detection	EIE	EB	EA	•	•	•	FB	FA

- Counter to set operation control, selection of detecting cycle and pullup/down registance option in case of using event-detecting function.
- It is able to output interrupt signal from EIRQ pin when detect from EINA for event detection and each pin of EINA. After detecting, detecting operation is automatically stopped and pulldown resistance is automatically connected. In case of restart detection, reseeting is needed. When detecting, detecting flag is set according to input pin, so that event detection with software is also possible.

* For details, see "9.4. Event detecting Function".

9.1.6. Down-counter for fixed cycle timer (Reg - C[h] ~ D[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
C	Timer Setup	TE	FE	TD1	TD0	2048	1024	512	256
D	Timer Counter	128	64	32	16	8	4	2	1

- Register to set up operation control, selection of clock cycle for timer and presetting value of timer in case of using timer interrupt function.

* For details, see "9.2. Event detecting Function".

9.1.7. Control register 1 (Reg - E[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
E	Control Register 1	•	•	•	TI / TP	AF	TF	AIE	TIE

- This register is used to record the result of various interrupt event detection operations, or to control the interrupt signal that is externally output when an interrupt event occurs.

1) TI / TP bit (Interrupt Signal Output Mode Select. Interrupt / Periodic)

When a fixed-cycle timer interrupt event occurs (when the TF bit goes from "0" to 1") , this bit specifies whether the interrupt operation occurs just once or repeatedly.
Writing "1" to this bit sets repeated operation.
Writing "0" to this bit sets single-shot operation.
* For details, see "9.2. Fixed-cycle Timer Interrupt Function ".

2) AF bit (Alarm Flag)

This is a flag bit that retains the result when an alarm interrupt event has been detected.
When an alarm interrupt event occurs, this bit's value changes from "0" to "1".
* For details, see "9.3. Alarm Interrupt Function".

3) TF bit (Timer Flag)

This is a flag bit that retains the result when a fixed-cycle timer interrupt event has been detected.
When a fixed-cycle timer interrupt event occurs, this bit's value changes from "0" to "1".
* For details, see "9.2. Fixed-cycle Timer Interrupt Function ".

4) AIE bit (Alarm Interrupt Enable)

This bit sets the operation of the /AIRQ interrupt signal when an alarm interrupt event has occurred (the AF bit value changes from "0" to "1").
When a "1" is written to this bit, occurrence of an interrupt event causes a low-level interrupt signal to be output from /IRQ pin.
Writing "0" to this bit prohibits low-level output from the /IRQ pin.
* For details, see "9.3. Alarm Interrupt Function".

5) TIE bit (Timer Interrupt Enable)

This bit sets the operation of the /IRQ interrupt signal when a fixed-cycle interrupt event has occurred (the TF bit value changes from "0" to "1").
When a "1" is written to this bit, occurrence of an interrupt event causes a low-level interrupt signal to be output from /IRQ pin.
Writing "0" to this bit prohibits low-level output from the /IRQ pin.
* For details, see "9.2. Fixed-cycle Timer Interrupt Function ".

9.1.8. Control register 2 (Reg - F[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
F	Control Register 2	○	TEST	0	RESET	HOLD	○	○	○

• This register is used to control stop and resume operations of the clock and calendar function, etc..

1) TEST bit

This is the manufacturer's test bit.
Always leave this bit value as "0" except when testing.
Be careful to avoid writing to this bit when writing "1" to other bits in this register.

* If this bit is inadvertently set (= "1") there is a safety function that auto-clears the TEST bit to zero when the CE0 pin or CE1 pin goes to low level.

2) RESET bit

Like the STOP function described above, this bit stops the counter operation and resets the internal counter when its value is less than one second.
Writing "1" to this bit stops the counter's operation and resets the RTC's internal counter when its value is less than one second.
Writing a "0" to this bit or setting the CE0 pin or CE1 pin to low level automatically clears (resets) this bit to zero.

* In case of RESET=1, in addition to event detecting function, counter function and almost all other functions are stopped.

3) HOLD bit

This bit pauses updating of the clock register. If sets HOLD=1 and read out date and hours data, it is surely able to read well-coordinated data.
Although, clock calendar data writing and taking up are overlapped so it is able to prevent data mismatching.
Writing "0" to this bit cancels pause mode (resumes clock updates). When HOLD is returned from "1" to "0", if an internal update has occurred in the meantime, an auto compensation function automatically performs a one-second clock update.

* Even if the time during which HOLD = "1" is two or more seconds, the auto compensation function only compensates the clock update by one second, so using the HOLD bit for one second or less is

recommended.

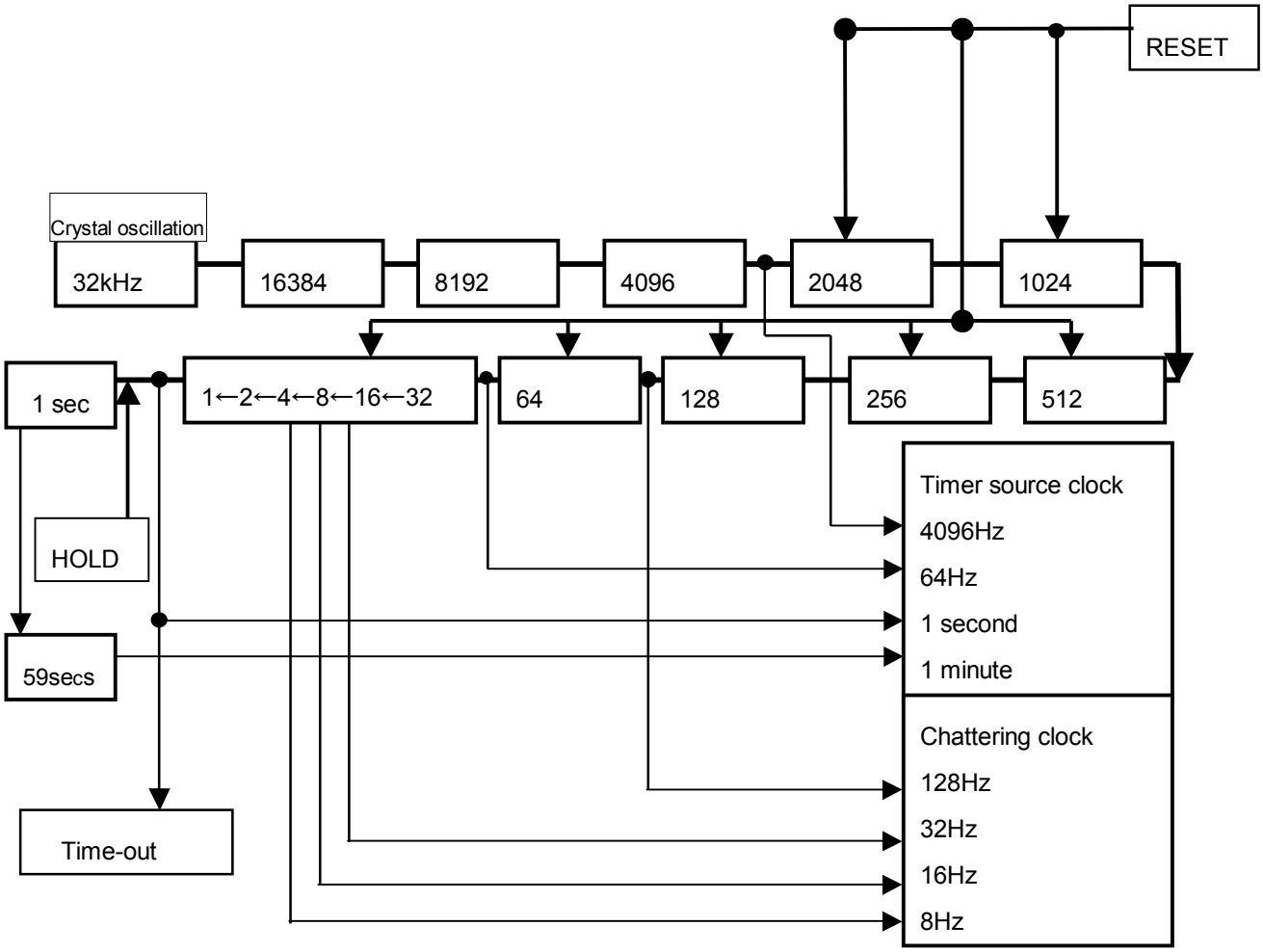
4) RESET, HOLD bit settings and operation of functions

bit		Function				
RESET	HOLD	Clock	Timer	Alarm	FOUT	Event Detection
0	0	runs	runs	runs	runs	runs
0	1	*1	*2	stops	runs	runs
1	0	stops	*3	stops	runs	stops
1	1	stops	*3	stops	runs	stops

*1: If the deviation is within one second, the automatic compensation function will kick in to perform the automatic compensation.
*2: Runs at source clock other than source clock at 1/60 Hz (1 min).
*3: Runs when the source clock is at 4096 Hz.
*4 : Correcting function for taking up with HOLD is also functioned when writing.
In case of writing access after HOLD setting, additional correcting for 1 second is executed after finishing access if taking up is occurred during access.

5) RESET, HOLD circuit block image

RESET zero works for resetting from 2048 to 1hz.
For this, not only timer except 4096Hz but also chattering free and time-out are not functioned during RESET.
1Hz clock of timer and time-out are runned even during HOLD but timer 1-minute clock is stopped because HOLD prohibits input signal into 1-miniute registers.
Similarly, chattering free function is not affected during HOLD.



9.2. Fixed-cycle Timer Interrupt Function

9.2.1. Fixed-cycle timer interrupt function related register

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
C	Timer Setup	**TE**	**FE**	**TD1**	**TD0**	**2048**	**1024**	**512**	**256**
D	Timer Counter	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
E	Control Register 1	•	•	•	**TI / TP**	AF	**TF**	AIE	**TIE**

∗ Before entering settings for operations, we recommend todo "0" clear to the TE and TIE bits to avoid unnecessary interrupt from occurring inadvertently while entering settings.

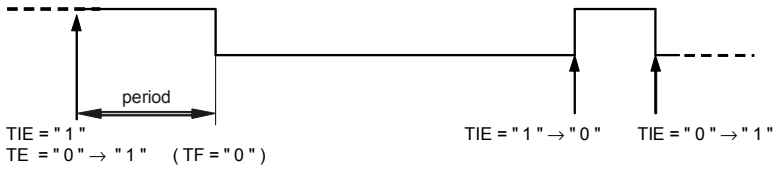
1) TI / TP bit (Timer Interrupt / Periodic)

When a fixed-cycle timer interrupt event occurs (TF value changes from "0" to 1"), this bit specifies whether the interrupt operation will be performed only once or repeatedly.

TI / TP	Data	Description
Write / Read	0	[Level interrupt mode] Makes operation of fixed-cycle timer interrupt function only once
	1	[Repeated interrupt mode] Makes continuous operation of fixed-cycle timer interrupt function repeatedly

∗**1)** Outline drawing of level interrupt mode (TI/TP = "0")
After an interrupt event occurs, the operation is performed only once.

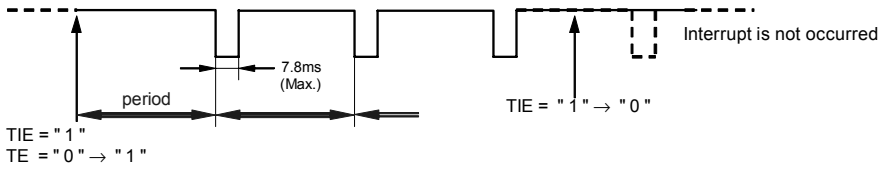
∗Example of /IRQ operation



∗**2)** Outline drawing of repeated interrupt mode (TI/TP = "1")

After an interrupt event occurs, the operation is performed repeatedly.

∗Example of /IRQ operation



2) TD1, TD0 bit

These bits specify the fixed-cycle timer interrupt function's countdown period (source clock).
Four different periods can be selected via combinations of these two bit values.

TD1, TD0	**TD1 (bit 5)**	**TD0 (bit 4)**	Source clock	Auto reset time tRTN
W / R	**0**	**0**	4096 Hz / Once per 244.14 μs	**122 μs**
	0	**1**	64 Hz / Once per 15.625 ms	**7.813 ms**
	1	**0**	1 Hz / Once per second	**7.813 ms**
	1	**1**	1/60 Hz / Once per minute	**7.813 ms**

∗1) The /IRQ pin's auto reset time (tRTN) varies as shown above according to the source clock setting.

∗2) An interrupt that occurs when the source clock is in 1/60 Hz mode is linked to the internal clock's "minute" update operation.

∗3) An interrupt that occurs when the source clock is in 1 Hz mode is not linked to the internal clock. (Instead, a dedicated 1 Hz timer circuit is used for independent operation.)

3) Down counter for fixed-cycle timer (Timer Counter)

This register (Reg-D) is used for setting up initial value (pre-setting value) of presettable down counter, and is able to set up optional cpount value from 1 (01 h) ~ 4095 (FFF h).
The counter counts down based on the source clock's period, and when the count value changes from 01h to 00h, the TF bit value becomes "1".

∗**1**. When start to read this cpount down, presetting value can always be read.
Count value during cound down cannot be read.

∗**2.** When the fixed-cycle timer interrupt function is not being used, this register b it can be used as a memory bit. But in such cases, unless stop time with setting to "0" to the TE and TIE, memory value may be changed due to data declimentation or unnecessary interrupt may be occurred.

4) TE bit (Timer Enable)

This bit enables operation of the fixed-cycle timer interrupt function to start.

TE	Data	Description
Write / Read	**0**	Timer is stopped after reloading presetting valu. It is unable to pausetimer even if set this bit to zero during count down.
	1	Fixed-cycle timer is counted down. With level interrupt mode, it is zero cleared simultaneously with interrupt occurrence. (Note) During level interrupt mode, the TF bit first should be cleared to zero, then the TE bit value should be changed from "0" to "1".

5) TF bit (Timer Flag)

This is a flag bit that retains the result when a fixed-cycle timer interrupt event is detected.

The value of this bit changes from "0" to "1" when a fixed-cycle timer interrupt event occurs. If the TIE bit value is “1" at that time, the /IRQ pin goes to low level to indicate that an event has occurred.

TF	Data	Description
Write	**0**	If execute " 0 " clear, external output of timer interrupt can be cancelled. However, during repeated intrrupt, it is unable to cancel since interrupt time is fixed.
	1	This bit is invalid after a "1" has been written to it.
Read	**0**	No timer interrupt occurrence.
	1	Timer interrupt events are detected. ∗ Result is retained until this bit is cleared to zero

6) TIE bit (Timer Interrupt Enable)

This bit sets the operation of the /IRQ interrupt signal when a fixed-cycle timer interrupt event has occurred (TF bit value changes from "0" to "1").

When a "1" is written to this bit, occurrence of an interrupt event causes a low-level interrupt signal to be output from /IRQ pin.
When a "0" is written to this bit, output from the /IRQ pin is prohibited (disabled).

TIE	Data	Description
Write / Read	**0**	1) When a fixed-cycle timer interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status remains Hi-Z). 2) When a fixed-cycle timer interrupt event occurs, the interrupt signal is canceled (/INT status changes from low to Hi-Z).
	1	When a fixed-cycle timer interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low).

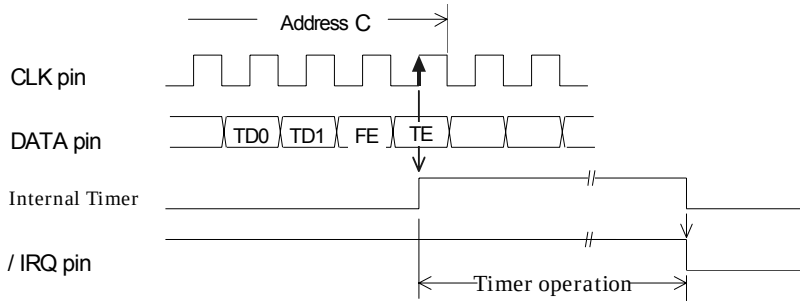
7) FE bit (FOUT Enable)

Bit to control 32768Hz output of FOUT pin.
It is able to control optional output in combination with FOE pin.

FE	FE value	FOE pin setting	FOUT pin condition
Write / Read	0	High	32768Hz output
		Low	Hi-Z
	1	High	32768Hz output
		Low	32768Hz output

9.2.2. Timer start timing

Counting down of the fixed-cycle timer value starts at the rising edge of the CLK signal that occurs when the TE value is changed from "0" to "1" (after bit 0 is transferred).



9.2.3. Fixed-cycle timer interrupt interval and time error

The combination of the source clock settings (settings in TD1 and TD0) and fixed-cycle timer countdown setting (Reg–C setting) sets the fixed-cycle timer interrupt interval, as shown in the following examples.

Timer Counter setting	Source clock			
	4096 Hz TD1,0 = 0,0	64 Hz TD1,0 = 0,1	1 Hz TD1,0 = 1,0	1/60 Hz TD1,0 = 1,1
0 (00h)	–	–	–	–
1 (01h)	244.14 μs	15.625 ms	1 s	1 min
2 (02h)	488.28 μs	31.250 ms	2 s	2 min
3 (03h)	732.42 μs	46.875 ms	3 s	3 min
• • •	• • •	• • •	• • •	• • •
4095 (FFFh)	999.75 ms	63.984 s	1h8min15s	2day 20h 15min

- Fixed-cycle timer interrupts time error and fixed-cycle timer interrupt interval time

A fixed-cycle timer interrupt time error is an error in the selected source clock's $^{+0}/_{-1}$ interval time. Accordingly, the fixed-cycle timer interrupt's interval (one cycle) falls within the following range in relation to the set time.

Fixed-cycle timer interrupt's interval

(Fixed-cycle timer interrupt's set time(∗) – source clock interval) to (fixed-cycle timer interrupt set time)

∗) Fixed-cycle timer interrupt's set time = Source clock setting × Countdown timer setting for fixed-cycle timer

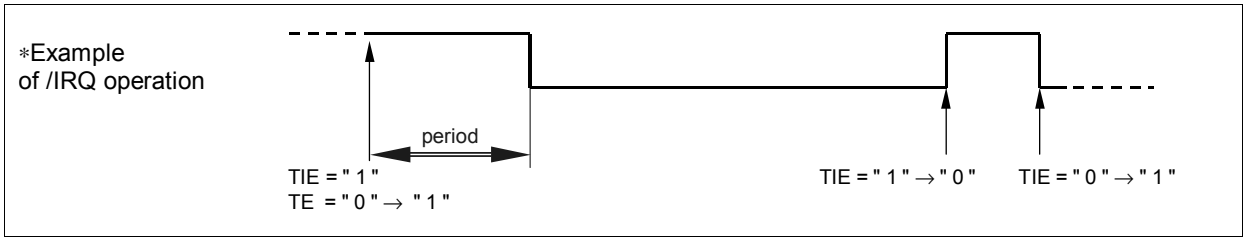
∗ The time actually set to the timer is adjusted by adding the time described above to the communication time for the serial data transfer clock used for the setting.

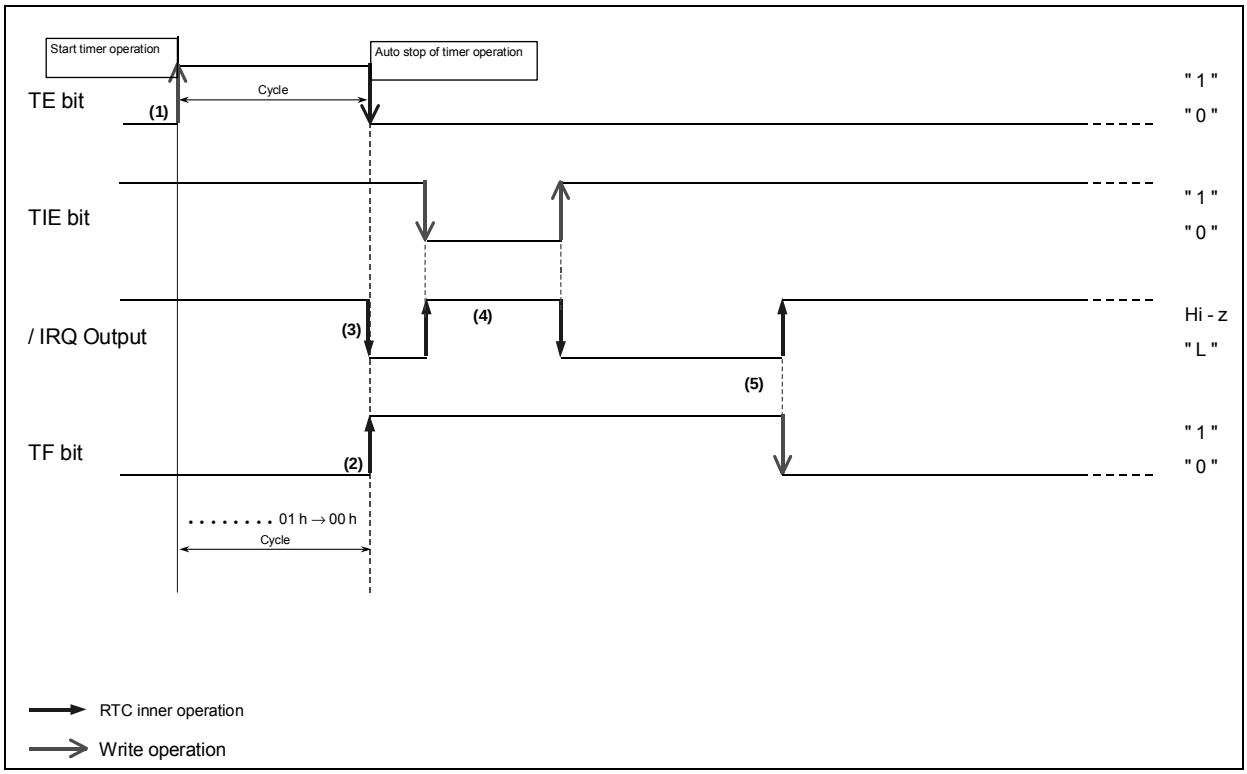
9.2.4. Diagram of fixed-cycle timer interrupt function

IRQ pin concerned, alarms interrupt and timer interrup are OR output.
Hereinafter, explain about timer interrupt on the assumption that no alarm interrupt is occurred.

9.2.4.1. Level interrupt mode (TI / TP = " 0 ")

- After an interrupt event has occurred, this function operates only once.





∗) Before using level interrupt mode (TI / TP = "0") , be sure to clear the TE bit and the TF bit to zero each time.

(1) When a "1" is written to the TE bit, the fixed-cycle timer countdown starts from the preset value.

(2) A fixed-cycle timer interrupt event starts a countdown based on the countdown period (source clock). When the count value changes from 01h to 00h, an interrupt event occurs.
At the same time, TE bit is zero cleared and preset value is loaded by timer cpunter to stop.

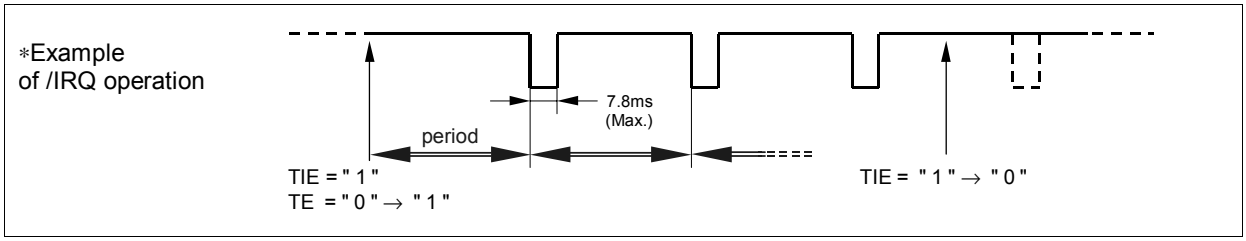
(3) If the TIE bit = "1" when a fixed-cycle timer interrupt occurs, /IRQ pin output goes low.
If TIE = " 0 ", /IRQ pin does not output timer interrupt.

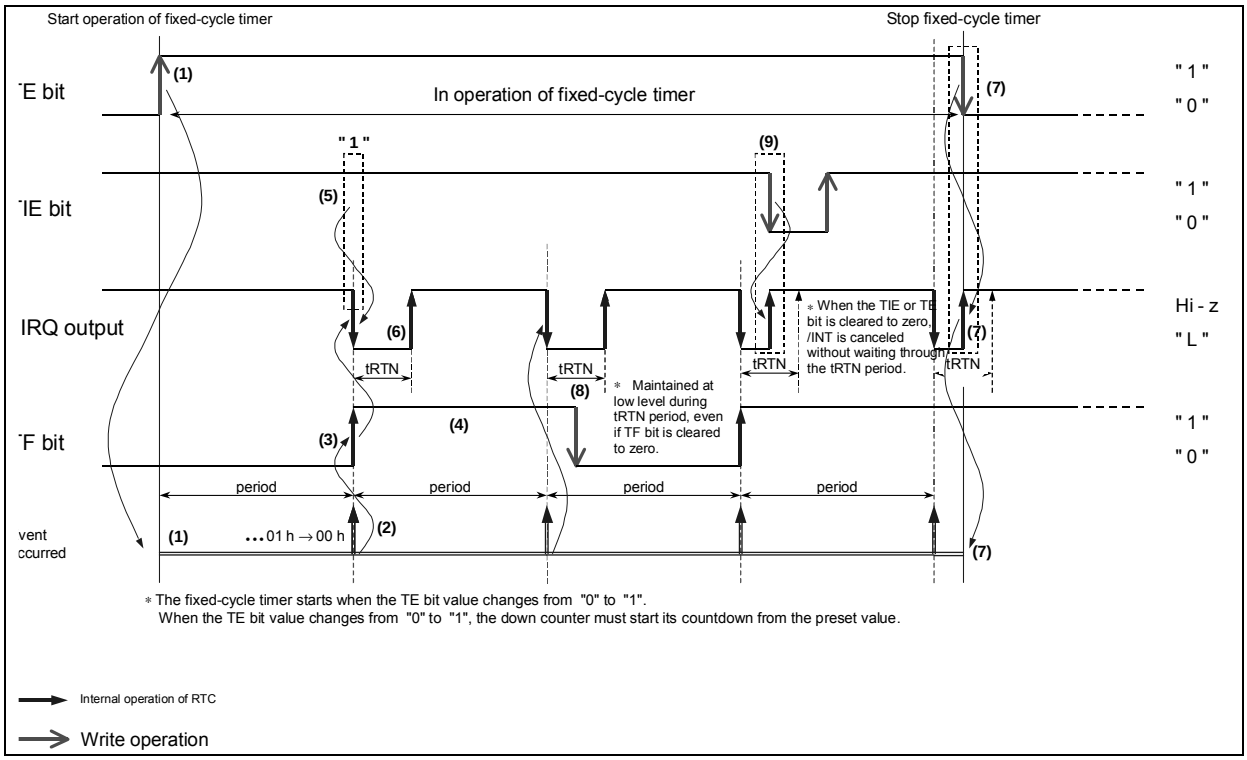
(4) During the period when the TF bit value is "1" following the occurrence of an interrupt event, the TIE bit can be set to switch the /IRQ pin to any status.

(5) When the TF bit = "1" its value is retained until it is cleared to zero.
If TF bit is cleared to " 0 ", output of timer interrupt is stopped.

9.2.4.2 Repeated interrupt mode (TI/TP = "1")

- With set cycle, execution of the operation is automatically repeated continuously.





(1) When a "1" is written to the TE bit, the fixed-cycle timer countdown starts from the preset value.

(2) A fixed-cycle timer interrupt event starts a countdown based on the countdown period (source clock). When the count value changes from 001h to 000h, an interrupt event occurs.
∗ After the interrupt event that occurs when the count value changes from 01h to 00h, the counter automatically reloads the preset value and again starts to count down. (Repeated operation)

(3) When a fixed-cycle timer interrupt event occurs, "1" is written to the TF bit.

(4) TF bit maintains " 1 " until it is cleared to zero.
(Even if cleare TE bit to zero, TF bnit is not affected.)

(5) If the TIE bit = "1" when a fixed-cycle timer interrupt occurs, /IRQ pin output goes low.
∗ If TIE =”0” when occurred fixed-cycle timer interrupt, timer interrupt does not output to /IRQ.

(6) Output from the /IRQ pin remains low during the tRTN period following each event, after which it is automatically cleared to Hi-Z status.
∗ /IRQ is again set low when the next interrupt event occurs.

(7) When a "0" is written to the TE bit, the fixed-cycle timer function is stopped and the /IRQ pin is set to Hi-Z status.

(8) When /IRQ is at low level and the TF is changed from "1" to “0”, / IRQ remains at low level and is not reset to Hi-Z status.

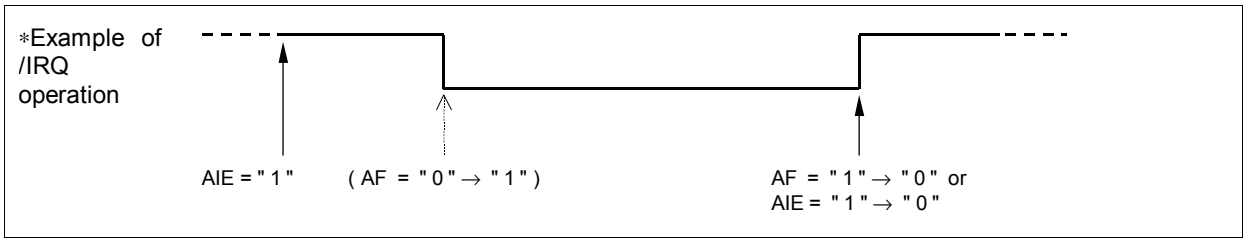
(9) When /IRQ = low, the /IRQ pin status changes from “1” to “0”, it changes from /IRQ “L” to Hi-z immediately.

9.3. Alarm Interrupt Function

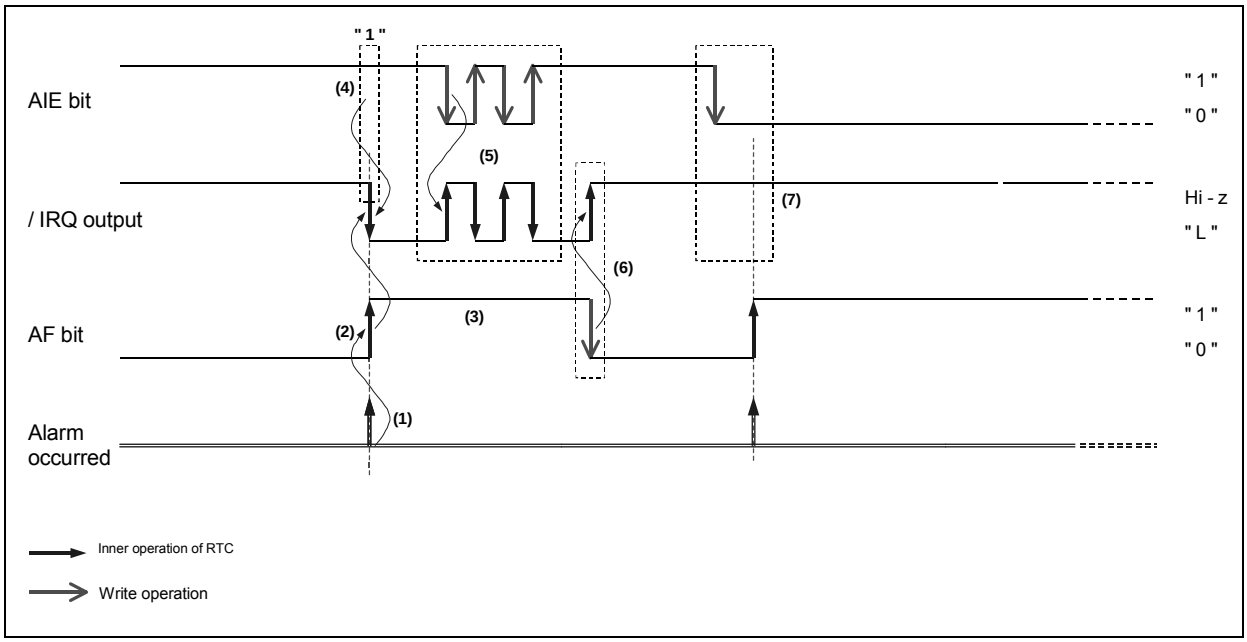
The alarm interrupt generation function generates interrupt events for alarm settings such as date, day, hour, and minute settings.

When an interrupt event occurs, the AF bit value is set to "1" and the /IRQ pin goes to low level to indicate that an event has occurred.

∗ /IRQ pin concerned, alarm interrupt and fixed-cycle timer interrupt execute OR output.
Hereinafter, explain about alarm interrupt on the assumption that no fixed-cycle timer interrupt is occurred.



9.3.1. Diagram of alarm interrupt function



(1) Comparison operation of the date/time and alarm is done with update timing when changed from 59 to 00 sec. Therefore, even if alarm data with the same as the present time is set, alarm will not be given immediately.

(2) When a time update interrupt event occurs, the AF bit values becomes "1".

(3) When the AF bit = "1", its value is retained until it is cleared to zero.

(4) If AIE = "1" when an alarm interrupt occurs, the /IRQ pin output goes low.
∗ When an alarm interrupt event occurs, /IRQ pin output goes low, and this status is then held until it is cleared via the AF bit or AIE bit.

(5) If the AIE value is changed from "1" to "0" while /IRQ is low, the /INT status immediately changes from low to Hi-Z. After the alarm interrupt occurs and before the AF bit value is cleared to zero, the /IRQ status can be controlled via the AIE bit.

(6) If the AF bit value is changed from "1" to "0" while /INT is low, the /IRQ status immediately changes from low to Hi-Z.

(7) If the AIE bit value is "0" when an alarm interrupt occurs, the /IRQ pin status remains Hi-Z.

9.3.2. Alarm interrupt function registers

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	MIN	fr	40	20	10	8	4	2	1
2	HOUR	fr	•	20	10	8	4	2	1
4	DAY	fr	•	20	10	8	4	2	1
7	MIN Alarm	AE	40	20	10	8	4	2	1
8	HOUR Alarm	AE	•	20	10	8	4	2	1
9	DAY Alarm	AE	•	20	10	8	4	2	1
E	Control Register 1	•	•	•	TI / TP	AF	TF	AIE	TIE

∗ Before entering settings for operations, we recommend writing a "0" to the AIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.

∗ When the alarm interrupt function is not being used, the Alarm registers (Reg - 7 to 9) can be used as a RAM register. In such cases, be sure to write "0" to the AIE bit.

∗ ∗ Even when the alarm registers (Reg - 7 to 9) are used as a RAM register, surely set AIE bit to “0” to avoid unnecessary alarm due to conincidence with write data and the present time.

1) Alarm registers (Reg - 7[h] ~ A[h])

Set hour, minute and date to be given alarm.

When the settings made in the alarm registers match the current time, the AF bit value is changed to "1". At that time, if the AIE bit value has already been set to "1", the /IRQ pin goes low.

∗1) Register set to AE = " 1 " concerned, it is always functioned as alarm agreement regardlessofdata.
(Example) Write 81h (AE = "1") to the DAY Alarm register (Reg - 9):
Alarm is given only due to coincidence with hour and minute data because date is always coincidence.

∗2) When set all 3 AE bits to " 1 " , alarm interrupt is occurred every minute.

∗3) Comparison of alarm is done in timing when update from 59 to 00 seconds.

2) AF bit (Alarm Flag)

This is a flag bit that retains the result when an alarm interrupt event has been detected.

When this flag bit value is already set to "0", occurrence of an alarm interrupt event changes it to "1".

AF	Data	Description
Write	0	The AF bit is cleared to zero to prepare for the next status detection * Clearing this bit to zero enables /IRQ low output to be canceled
	1	This bit is invalid after a "1" has been written to it.
Read	0	No alarm interrupt events are detected
	1	Alarm interrupt events are detected. * Result is retained until this bit is cleared to zero.

3) AIE bit (Alarm IRQ Interrupt Enable)

This bit sets the operation of the /IRQ interrupt signal when an alarm interrupt event occurs (when the TF bit value changes from "0" to "1").

Writing "1" to this bit causes a low-level interrupt signal to be output from the /IRQ pin when an interrupt event occurs.
When a "0" is written to this bit, output from the /IRQ pin is prohibited.

AIE	Data	Description
Write / Read	0	1) When an alarm interrupt event occurs, an interrupt signal is not generated (/IRQ status remains Hi-Z). 2) When an alarm interrupt event occurs, the interrupt signal is canceled (/IRQ status changes from low to Hi-Z).
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/IRQ status changes from Hi-Z to low).

∗ To detect occurrence of an alarm interrupt event without setting /IRQ to low level, monitor the AF bit value (note when it changes from "0" to "1") while AIE = "0".

9.3.3. Examples of alarm settings

1) Basic information about alarm settings

- Four parameters can be set as alarm objects are the following 3 items: minute, hour, day, and date.
- Hour settings are based on the round –the-clock system.
- Alarm register set AE bit to " 1 " is always considered alarm coincidence.
  If set AE to [date] and set alarm to 22:30 hours, alarms interrupt is occurred at 22:30 hrs every day since date is disregarded.

∗ When the AE bit = 1 for all objects (minute, hour, day, and date), an alarm interrupt event is given every minute.

2) Examples of alarm settings are listed below.

Examples of alarm settings	Reg - 9 DAY Alarm	Reg - 8 HOUR Alarm	Reg - 7 MIN Alarm
•Gives alarm on 17th day at 07 : 00 [Dat] 17 [Hour] 07AM (round-the-clock system→07hour) [Minute] 00 minute orignored	17 h	07 h	80h ~ FFh AE = " 1 "
• Gives alarm at every minute sharp [Date] Ignored [Hour] Ignored [Minute] Ignored	80h ~ FFh AE = " 1 "	80h ~ FFh AE = " 1 "	80h ~ FFh AE = " 1 "

9.4. Event detecting functions

9.4.1. Event detection setting register

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
A	Input Setup	T1	T0	HLB	HLA	UDB	REB	UDA	REA
B	Event detection	EIE	EB	EA	•	•	•	FB	FA

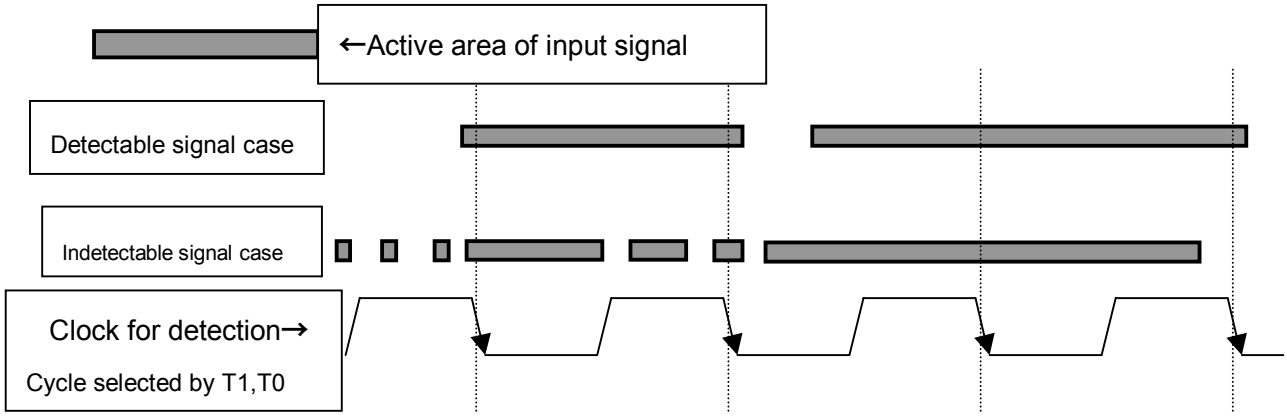
9.4.2. Setting bit functions related event detection

Port	BIT	Value	Function Specification
A	HLA	1	Set EINA pin to Hi input detection mode
		0	Set EINA pin to Low input detection mode
B	HLB	1	Set EINB pin to Hi input detection mode
		0	Set EINB pin to Low input detection mode
A	UDA	1	Inner resistance of EINA pin concerned, pullup side is effective.
		0	Inner resistance of EINA pin concerned, pulldown side is effective
			If detect input of EINA pin, UDA bit is automatically cleared to zero to make pulldown resistance effect. After input initial power, keeps zero clear condition.
	REA	1	Connect inner pullup/pulldown resistance to EINA pin.
		0	Release inner pullup/pulldown resistance of EINA pin
			If detect input of EINA pin, REA bit is automatically set and make a built-inresistance to ON. After input initial power, keeps set condition. In case a buil-in resistance is not used, through current is occurred if port input become to open and current consumption may be increased substantially.
B	UDB	1	Inner resistance of EINB pin concerned, pullup side is effective.
		0	Inner resistance of EINB pin concerned, pulldown side is effective.
			If detect input of EINB pin, UDB bit is automatically cleared to zero to make pulldown effect. After input initial power, keeps zero clear condition.
	REB	1	Connect inner pullup/pulldown resistance to EINB pin.
		0	Release inner pullup/pulldown resistance of EINB pin.
			If detect input of EINB pin, REB is automatically set to make a built-in Resistance ON. After input initial power, keeps set condition. In case a buil-in resistance is not used, through current is occurred if port input become to open and current consumption may be increased substantially.
A	FA	1	Input to EINA pin is detected. After setting, keeps “1” until 0-write.
		0	No input to EINA p;in.
B	FB	1	Input to EINB pin is detected. After setting, keeps “1” until 0-write.
		0	No input to EINB pin.
A	EA	1	Do detecting operation of EINA pin.
		0	Stop detection of EINA pin.
			If detect input of EINA pin, EA bit is automatically cleared to zero to stop Input detecting operation. To restart detection, resetting is needed. Inputdetection flag is still remained. After input initial power, keeps zero clear condition.
B	EB	1	Do detecting operation of EINB pin.
		0	Stop detection of EINB pin.
			If detect input of EINA pin, EB bit is automatically cleared to zero to stop Input detecting operation. To restart detection, resetting is needed. Inputdetection flag is still remained. After input initial power, keeps zero clear condition.
–	EIE	1	Accepts interrupt output when detect event.
		0	Prohibits interrupt output when detect event.
			Set interrupt output of OR result for flag A and flag B to accept or prohibit.

9.4.3. Setting of event detection cycle and reaction time of detection

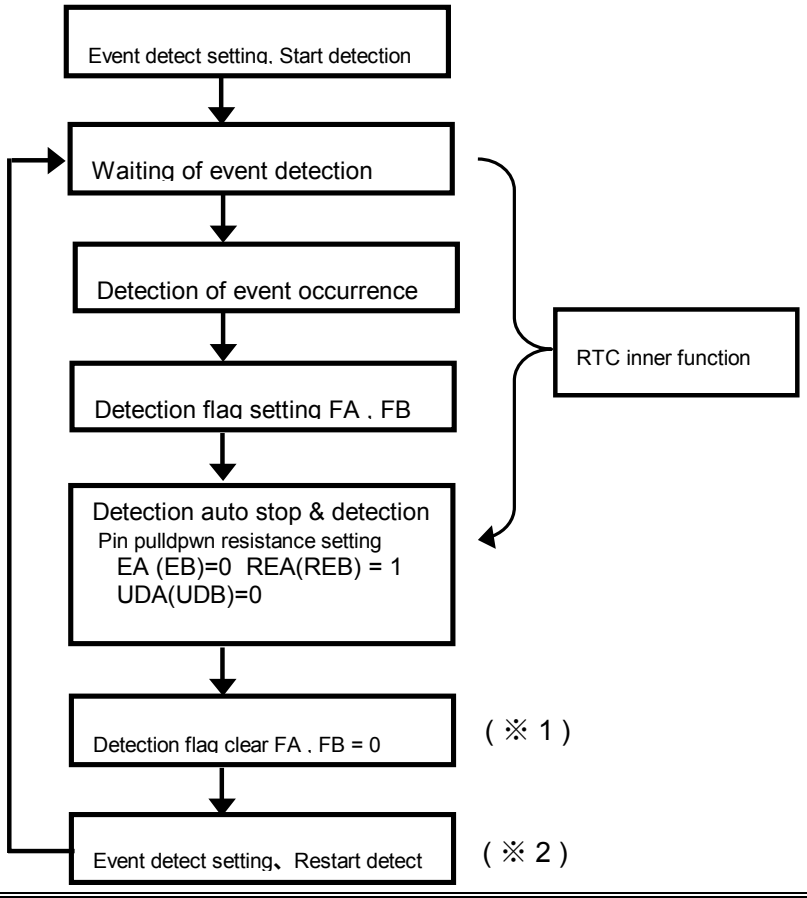
T1	T0	Event Detection Cycle (ms)
1	1	7.8
1	0	31.25
0	1	62.5
0	0	125.0

Operating image of detection timing and input chattering removal



Input and judge if input signal is overlapped 2 continuous edge of detection timing clock.

9.4.4. Sample for setting procedure of event detection and notice for setting. Refer to the figure below.
After detecting event、※**1** after flaf cleared ※**2** implement restart setting of detection.
Ifrestart detecting operation first, flag clear processing is given priority in case flag clear and event occurrences are overlapped and event detection may be omitted.



9. 5. Setting of Interrupt Expansion Function

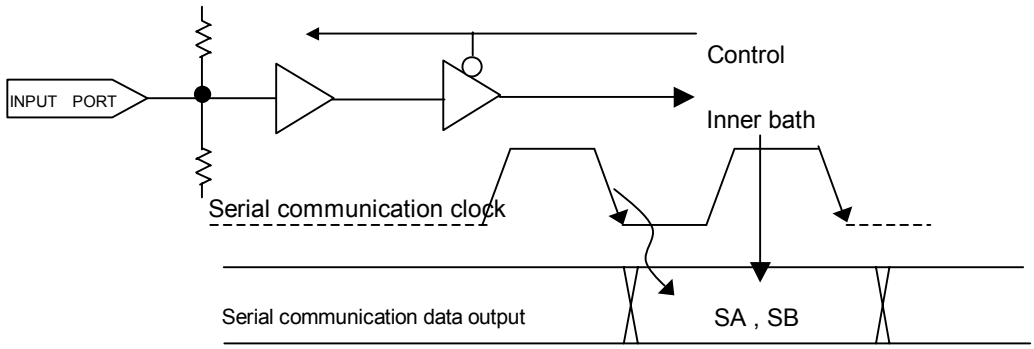
9.5.1 Register of interrupt expansion function

Address		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
3	Interrupt Setup	**fr**	**MIE**	**SB**	**SA**	**AOF**	**TOF**	**AQ**	**TQ**

■Register **3** Interrupt Setup Register description

BIT	Function	R/W	Value	Description
f r	Flag in taking up	**R**	**1**	Clock calendar register is in data update (it is not affected to R/W of this register)
	Read frag		**0**	Date/time registe is not in time update.
MIE	Multi interrupt setting bit	**R/W**	**1**	Accepts alarm timerinterrupt to output to EIRQ pin
	Multiple Interrupt Enable		**0**	Prohibits output to /EIRQ of alarm timer interrupt
SB	Event B port Monitor bit	**R**	**1**	Event input B port is Hi
	Status B port		**0**	Event input B port is Low
SA	Event A port Monitor bit	**R**	**1**	Event input A port is Hi
	Status A port		**0**	Event input A port is Low
AOF	Alarm interrupt Time-out flag	**R/W**	**1**	Alarm interrupt is timeout Unable to write 1 to AOF
	Alarm time out Flag.		**0**	No timeout of alarm interrupt Only zero clearis possible to write to AOF
TOF	Timer interrupt Time-out flag	**R/W**	**1**	Timer interrupt is timeout Unmable to write 1 to TOF
	Timer time out Flag.		**0**	No timeout of timer interrupt Only zero clear is possible to write to TOF
AQ	Alarm interrupt system Setting bit	**R/W**	**1**	Set alarm to timeout mode AF bit is automatically cleared 3 to 4 seconds after giving alarm and cancel interrupt output When timeout, AOF bit is set
	Alarm interrupt mode select		**0**	Alarm interrupt is not timeout
TQ	Timer interrupt system Setting bit	**R/W**	**1**	Set timer interrupt to timeout mode TF bit is automatically cleared 3 to 4 seconds after occurredtimer interrupt and cancel interrupt output When timeout, TOF bit is set In case of TI/TP=1, timeout function is not worked
	Timer interrupt mode select		**0**	Timerinterrupt is not timeout

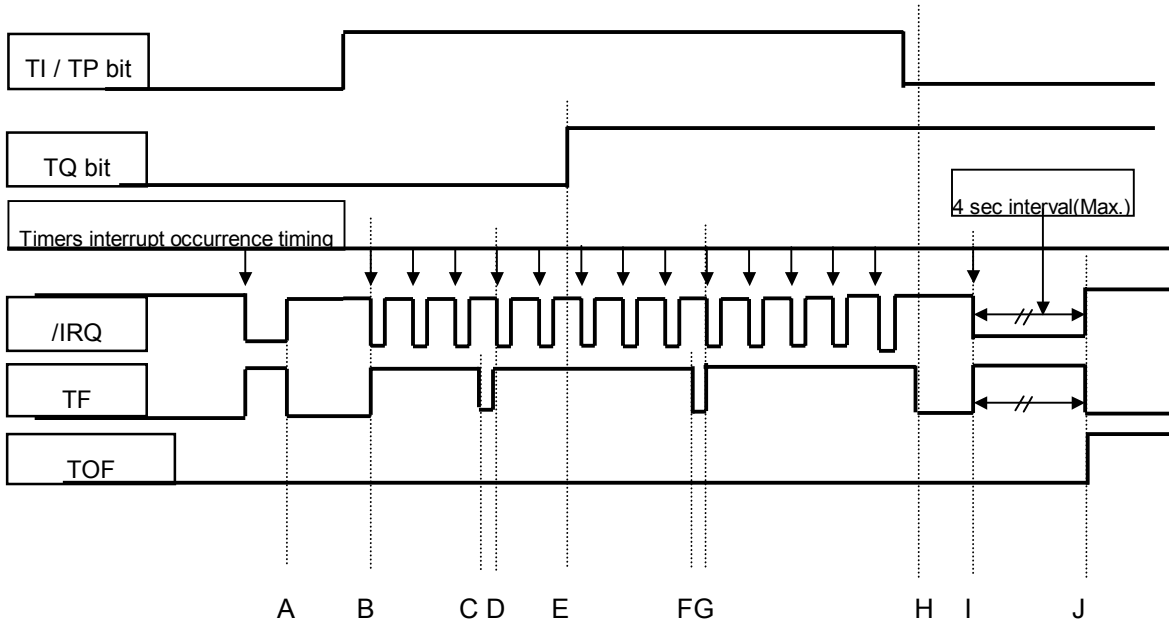
RX-4575 Monitor bit of event input port SA,SB bit circuit image



Latches status of input port with edge timing of the above serial communication clock.
In case input port data is in changing, output HI or Low.

9.5.2. Interrupt operation timing chart

Additional explanations of timer timeout mode operation



A：After occurred single interrupt of timer, TF clear is done and canceled interrupt.

B：After timer started operation with repeat interrupt mode, initial interrupt is occurred.

C：Cleared timer flag.

D：Interrupt is occurred and timer flag is set.

E：Set timer to timeout mode, but timeout function is not worked since continuous interrupt mode.

F：Cleared timer flag.

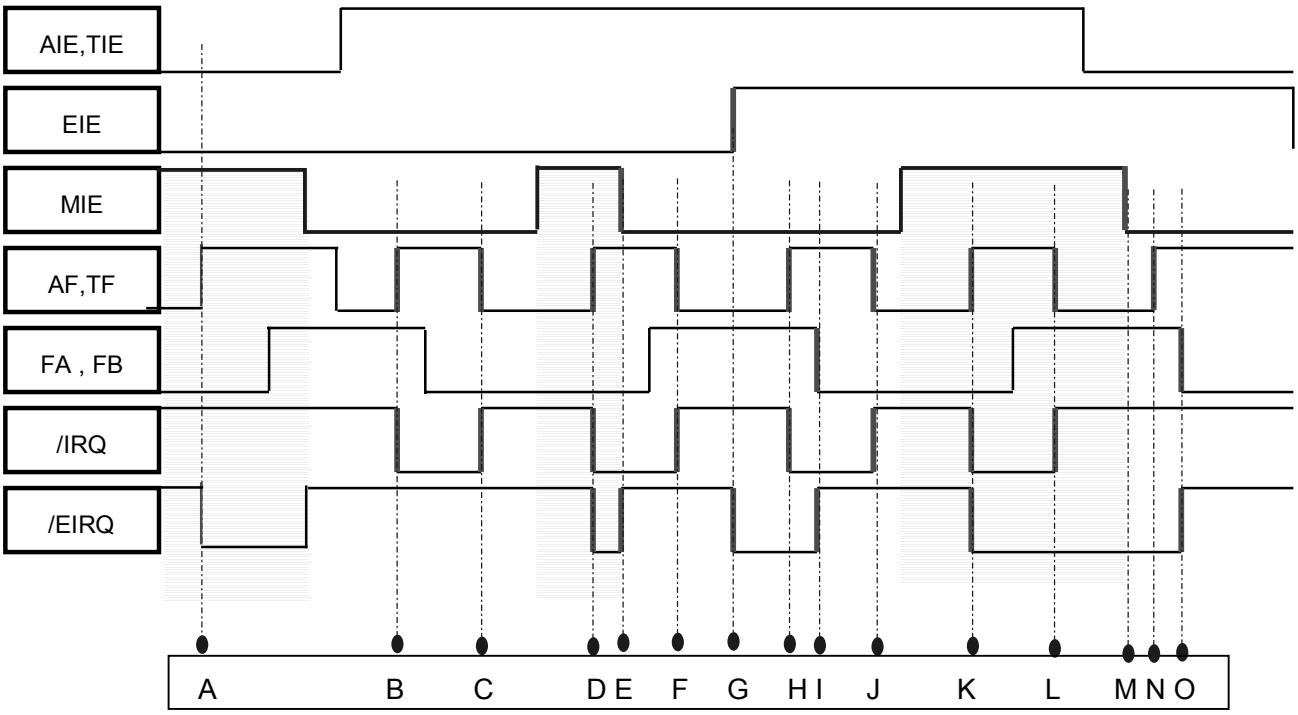
G：Even if interrupt is occurred, timer flag is set.

H：Cleared timer flag. Timer is single moder and timeout mode is effective.

I ： New single mode interrupt is occurred.

J ：Timer flag is cleared about 4 seconds after timeout without waiting flag clear and IRQ is cancelled. Timeout flag is set at the same time.

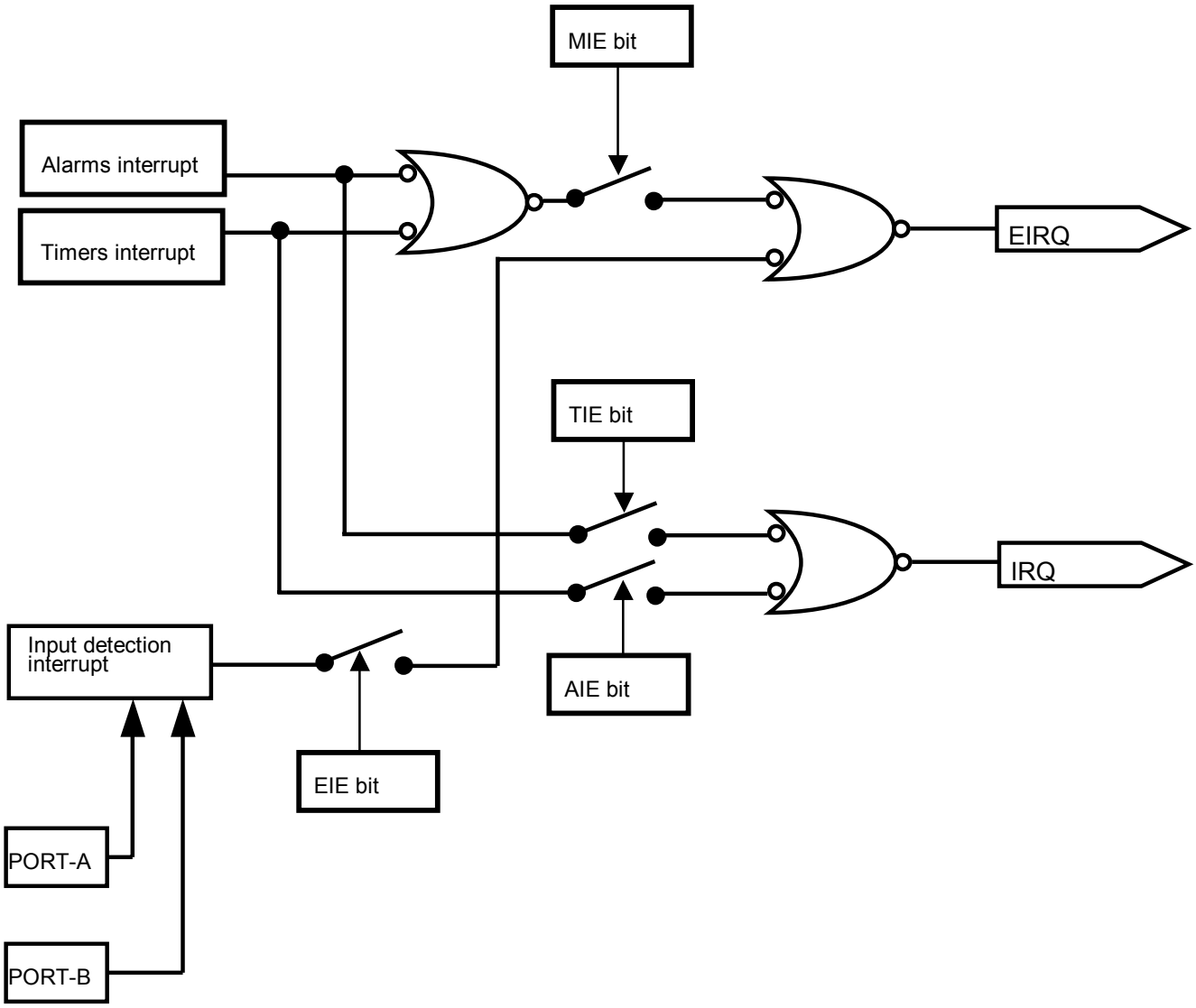
9.5.3 Additional explanations of interrupt operation with AIE, TIE, EIE, MIE



A：Even if AIE and TIE are zero, AF and TF are output to /EIRQ by MIE.
B：Only /IRQ acts LOW by AF,TF and AIE,TIE.
C：/IRQ is cancelled by AF and TF.
D：Both /IRQ and /EIRQ act LOW by AF,TF and AIE and MIE.
E：Only /EIRQ is cancelled by means of MIE clear.
F：/IRQ is cancelled by means of AF,TF clear.
G：With FA,FB setting by event detection, /EIRQ acts LOW by EIE setting.
H：/IRQ acts LOW by AF,TF and AIE,TIE.
/EIRQ maintains LOW by FA, FB and EIE.
I： /EIRQ is cancelled by FA,FB clear.
J： Same as C.
K：Same as D.
L：Only /IRQ is cancelled by AF,TF clear.
M：/EIRQ acts LOW because event interrupt is occurred even if cleared MIE.
N： Interrupt does not output from /IRQ because AIE, TIE are zero even if AF,TF are set.
O： Same as **I**.

9.5.4. Operation image of interrupt control circuit

Operation image of interrupt control bit is shown in the following sketch. But it is not actual circuit block.



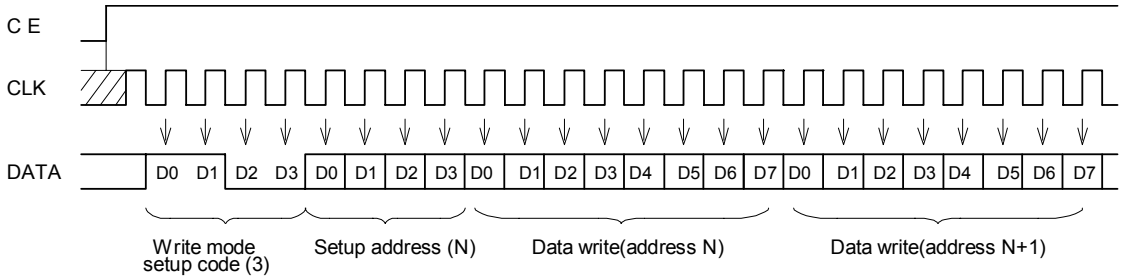
9.6. Read/Write of data

For both read and write, first set up 4-bits mode after starting up CE input, then specify the 4-bits address, and finally read or write in 8-bits units.

Both read and write use LSB-first. In continuous operation, objected address is auto incremented.
Auto incrementing of the address is cyclic, so address "F" is followed by address "0".

9.6.1. Write of data

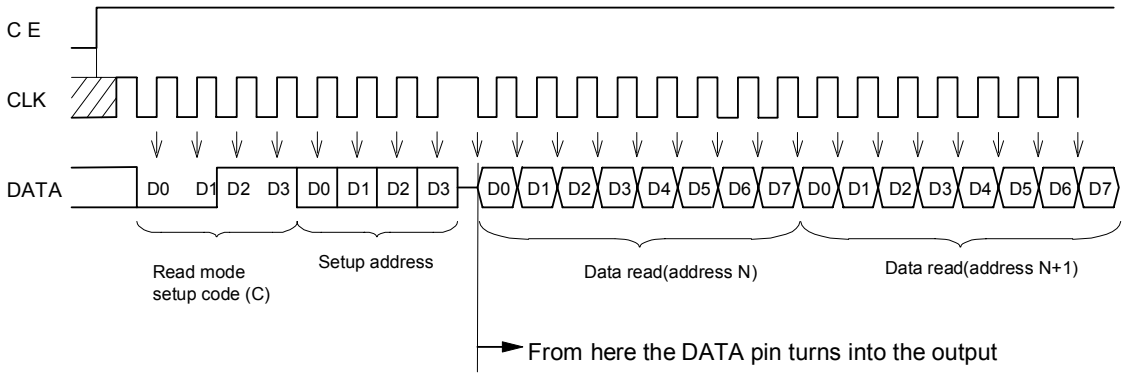
1) Take "3" as the write mode in the first four bits after the CE input rise, and set the address to write to the next four bits.
2) The next 8 bits of write data is written to the address set earlier, and the next 8 bits of data is written to the address which is automatically incremented from the last one.



※ When writing data, the data needs to be entered in 8-bits units.
If shut down CEO pin (or CEI pin) input before the input of data in 8-bits unit is not completed, the 8-bits data when CE input has shut down will not be written properly.

9.6.2. Read of data

1) Take "C" as the read mode in the first four bits after the CE input rise, and set the address to read to the next four bits.
2) The next 8 bits of read data is read from the address set earlier, and the next 8 bits of data is read from the address which is automatically incremented from the last one.



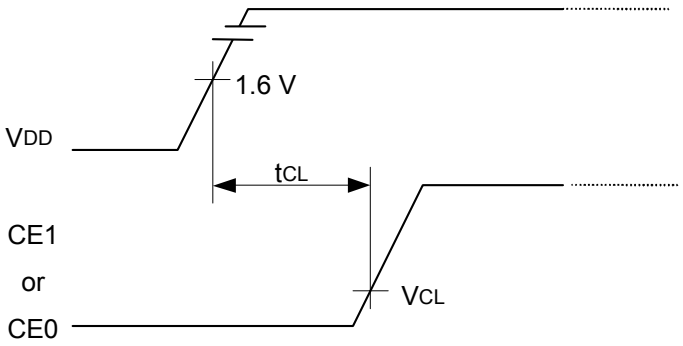
9.6.3. Mode setting code

Mode	Setting Code
Write	3 h
Read	C h

* In the mode setting code, if a value other than those listed above is used, the subsequent data will be ignored and the DATA pin remains in the input state.

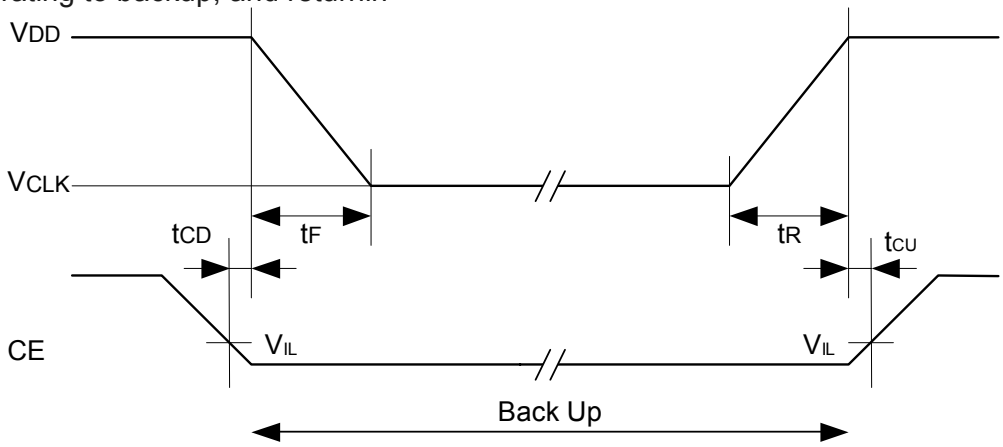
9.7. VDD and CE timing when supply power

※ When the power is turned to ON, use with CE = " L " (V_{CL}[V] in the diagram) as illustrated in the following timing
chart.
Pin with CE = " L " concerned, it may use either CE0 pin or CE1 pin only.



Item	Symbol	Remark	Specification	Unit
CE voltage when power is turned to ON	V_{CL}	CE impressed voltage until V_{DD} = 1.6 V	0.3 (Max.)	V
CE=V_{CL}[V] time when power is turned to ON	t_{CL}	Time to maintain CE=V_{CL}[V] until V_{DD} = 1.6 V	30 (Min.)	ms

9.8. Migrating to backup, and returnin



Item	Symbol	Condition	Min.	Typ.	Max.	Unit
CE time before power shutting down	t_{CD}	–	0			μs
Power shutting down time	t_F	–	2			μs / V
Power starting up time	t_R	–	25			μs / V
CE time after power starting up	t_{CU}	–	0			μs

9. 9 Access operation limit when supply initial power and backup returning

- Many operations of the products are interlocked to oscillation clock of a built-in crystal oscillator, therefore almost all functions are not worked if inner crystal oscillation is stopped.
  And calendar function, alarm, timer and event detection functions are also not worked.

  For this reason, we recommend to execute initial setting up from condition that oscillation is stopped due to some reason when supply initial power or dropping of voltage after starting of a built-in crystal oscillation and stabilizing IC inner functions.
  Concerning oscillation start time, please refer to oscillation starting time characteristic in item 6 frequency characteristic.

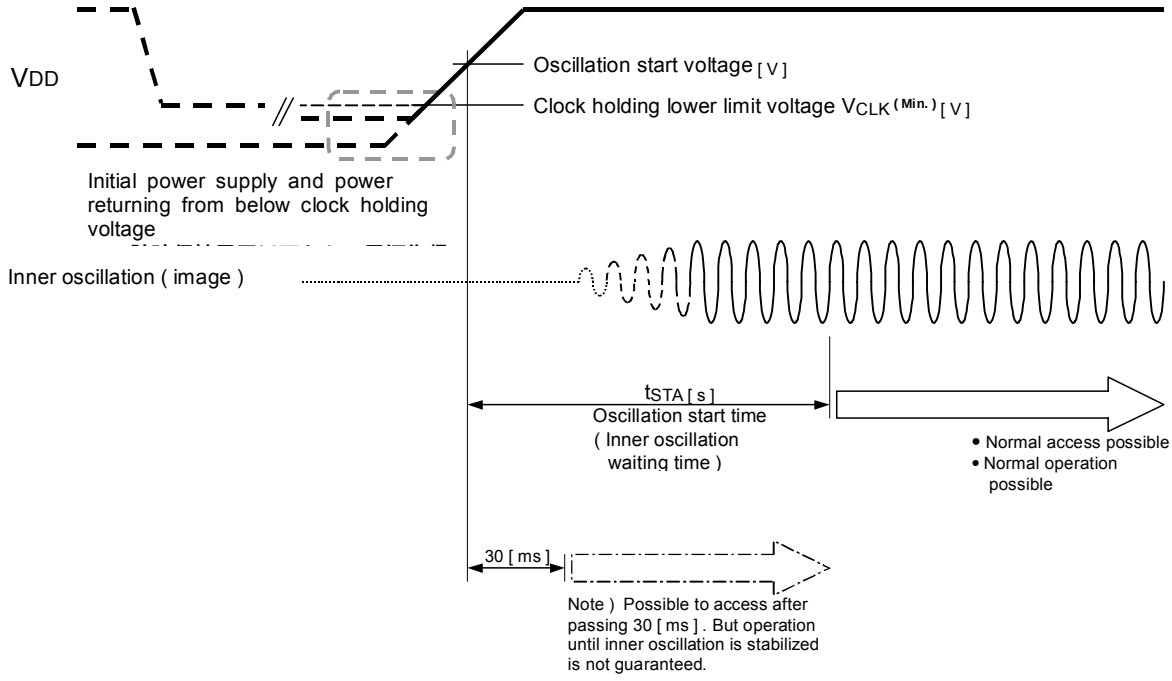
- Access operations when supply initial power and when returns power voltage from backup condition (hereinafter says "when transfer operation voltage") concerned, please pay attention to the followings.

  1) When transfer voltage, read fos-bit of second register first.

  2) If read result of fos-bit is " 1 ", initial seeting up for all registers are needed.
  If fos is "1", we recommend to do initial setting after oscillation started and inner oscillation is stabilized.

The condition when read fos-bit as " 1 " is as follows and initial setting is needed in any case. Condition 1) when supply first initial power. Condition 2) clock details may be lost due to voltage dropping in backup.

∗ Possible to access timing when supply initial power and return power voltage from below clock holding voltage.



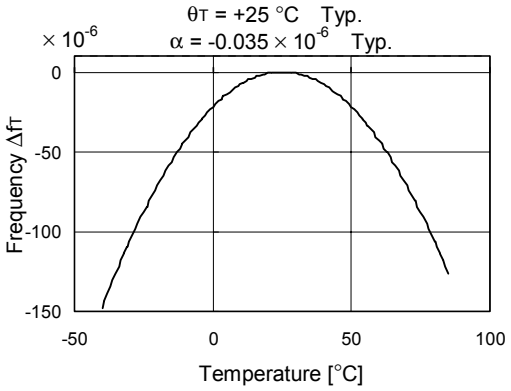
  3) Only in case read result of fos-bit is fos = " 0 (normal condition) " , possible to access without waiting oscillation start time.

The condition when read fos-bit as " 0 " is as follows, and it is possible to have normal operation. Condition 1) in case normal initialization is already done. Condition 2) when transfer operation voltage from backup condition, date is saved properly.

10 Reference information

10.1. Reference Data

(1) Example of frequency and temperature characteristics



[Finding the frequency stability]

1. Frequency and temperature characteristics can be approximated using the following equations.

   $\Delta f_T = \alpha (\theta_T - \theta_X)^2$

   - Δf_T : Frequency deviation in any temperature
   - α [1 / °C^2] : Coefficient of secondary temperature (-0.035 ± 0.005) $\times 10^{-6}$ / °C^2
   - θ_T [°C] : Ultimate temperature ($+25 \pm 5$ °C)
   - θ_X [°C] : Any temperature

2. To determine overall clock accuracy, add the frequency precision and voltage characteristics.

   $\Delta f/f = \Delta f/fo + \Delta f_T + \Delta f_V$

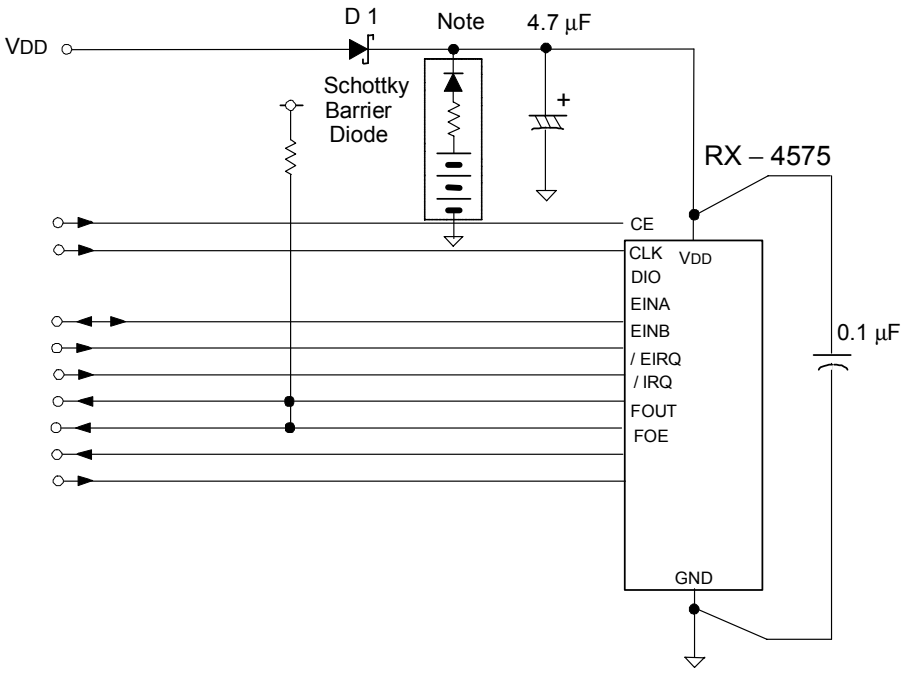
   - $\Delta f/f$: Clock accuracy (stable frequency) in any temperature and voltage.
   - $\Delta f/fo$: Frequency precision
   - Δf_T : Frequency deviation in any temperature.
   - Δf_V : Frequency deviation in any voltage.

3. How to find the date difference

   Date Difference = $\Delta f/f \times$ 86400(Sec)

   * For example: $\Delta f/f = 11.574 \times 10^{-6}$ is an error of approximately 1 second/day.

10.2. External connection example



Note :

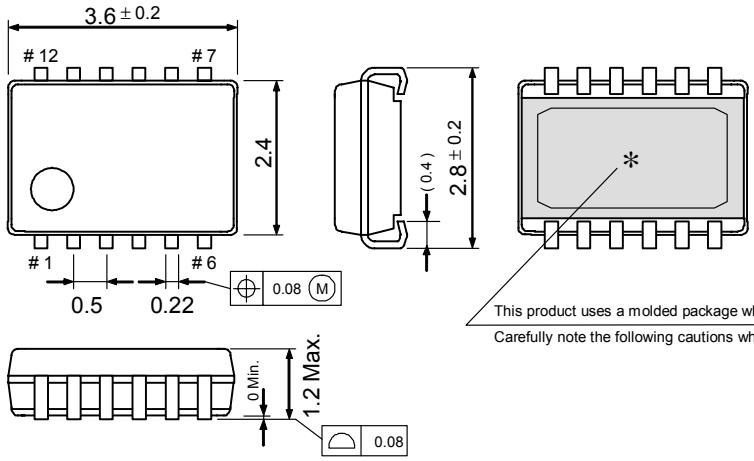
It uses the secondary battery or a lithium battery. When using the seconding battery, the diode is not required. When using the lithium battery, the diode is required. For detailed value on the resistance, please consult a battery maker.

11. External measurements / Marking layout

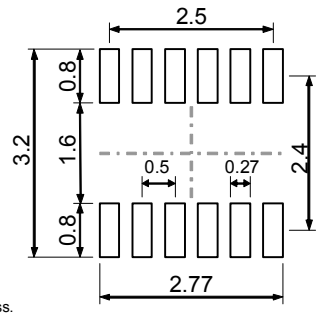
11.1. External measurements

RX – 4575 LC (VSOJ – 12pin)

- External measurements



- Recommended soldering patterns



Unit : mm

* Notes on packaging

This product uses a molded package whose back contains glass.
Carefully note the following cautions when handling.

(1) Packaging equipment

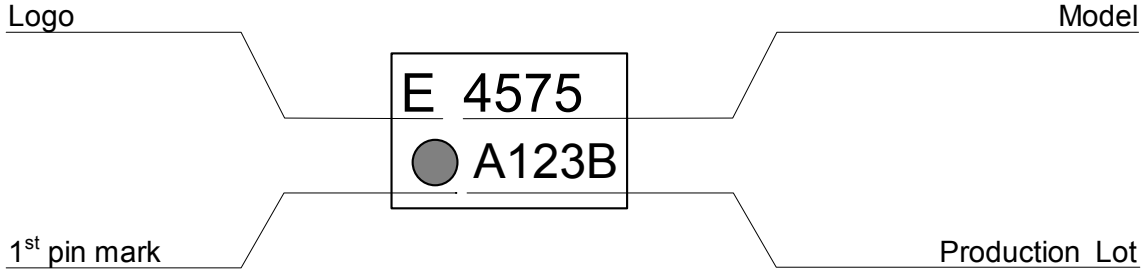
This product uses a molded package whose back contains glass.
Therefore, it is possible for shocks during packaging to cause product breakage, depending on the packaging machinery and conditions.
Please be sure to check that the load placed on products during packaging is as low as possible (low speeds during loading onto the substrate, low chuck forces, etc.) before using packaging equipment.
Carry out the same checks when changing packaging conditions.
The presence of foreign objects between this product and the packaging substrate may result in product breakage.
Guard against introduction of foreign objects during packaging.
Also, carry out measures to eliminate static electricity during packaging of and operations with this product.

(2) Stop using the glue

Any glue must never use it after soldering RTC to a circuit board.
This product has glass on the back side of a package.
When glue invasions between circuit board side and glass side, then glass cracks by thermal expansion of glue.
In this case a crystal oscillation stops.
Consider glue abolition or glue do not touch to RTC.

11.2. Marking layout

RX – 4575 LC (VSOJ – 12pin)



* The above informations are summary of seal and indication, and are not prescribed letterforms, sizes and positions.

12. Application notes

1) Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1 μF as close as possible to the power supply pins (between VDD and GNDs). Also, avoid placing any device that generates high level of electronic noise near this module.
* Do not connect signal lines to the shaded area in the figure shown in Fig. 1 and, if possible, embed this area in a GND land.

(3) Voltage levels of input pins

When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to VDD or GND.

(4) Handling of unused pins

Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, pull-up or pull-down resistors should be provided for all unused input pins.

2) Notes on packaging

(1) Soldering heat resistance.

If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.
* See Fig. 2 profile for our evaluation of Soldering heat resistance for reference.

(2) Packaging equipment

This product uses a molded package whose back contains glass.
Therefore, it is possible for shocks during packaging to cause product breakage, depending on the packaging machinery and conditions.
Please be sure to check that the load placed on products during packaging is as low as possible (low speeds during loading onto the substrate, low chuck forces, etc.) before using packaging equipment.
Carry out the same checks when changing packaging conditions.
The presence of foreign objects between this product and the packaging substrate may result in product breakage.
Guard against introduction of foreign objects during packaging.
Also, carry out measures to eliminate static electricity during packaging of and operations with this product.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

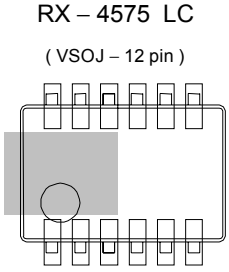
(5) Leakage between pins

Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

(6) Stop using the glue

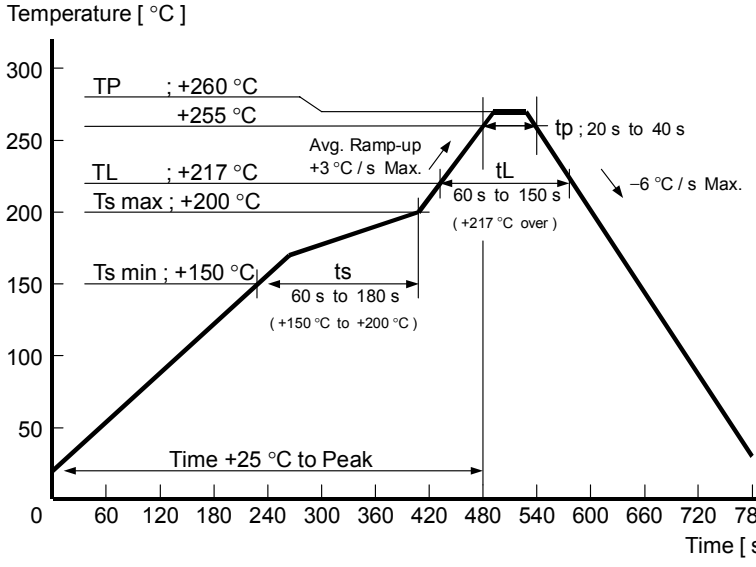
Any glue must never use it after soldering RX-4575LC to a circuit board.
RX-4575LC has glass on the back side of a package.
When glue invasions between circuit board side and glass side, then glass cracks by thermal expansion of glue.
In this case a crystal oscillation stops.
Consider glue abolition or glue do not touch to RX-4575LC.

Fig. 1 : Example GND Pattern



∗ The shaded part ( ) indicates where a GND pattern should be set without getting too close to a signal line

Fig. 2 : Reference profile for our evaluation of Soldering heat resistance.



EPSON TOYOCOM

Application Manual

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