AH-6120LR EB02 /
AP-6110LR EB02
Operation manual

(Evaluation Board for 6-Axis Motion Sensor and Analog Front End IC)

Seiko Epson Corporation
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NOTICE

Contents

Part 1 : Hardware section

Part 2 : Interface section

Part 1 : Hardware section

1. Feature

AH-6120LR EB02 or AP-6110LR EB02 is an evaluation board which carries motion sensor (AH-6120LR or AP-6110LR) and Analog Front End IC (S1A15001).

It has SPI interface terminal to connect external microcontroller to evaluate as a motion sensor module with digital output and/or a motion sensor.

I/F Signal terminal: XCS, SCLK, DOUT, DIN, DE

Power supply: VDDI, VDD, VSS

Sampling rate: 977 sps (clock frequency 2.0MHz.)

It is possible to input clock externally 2.048MHz to achieve 1k samples per second.

2. Block Diagram

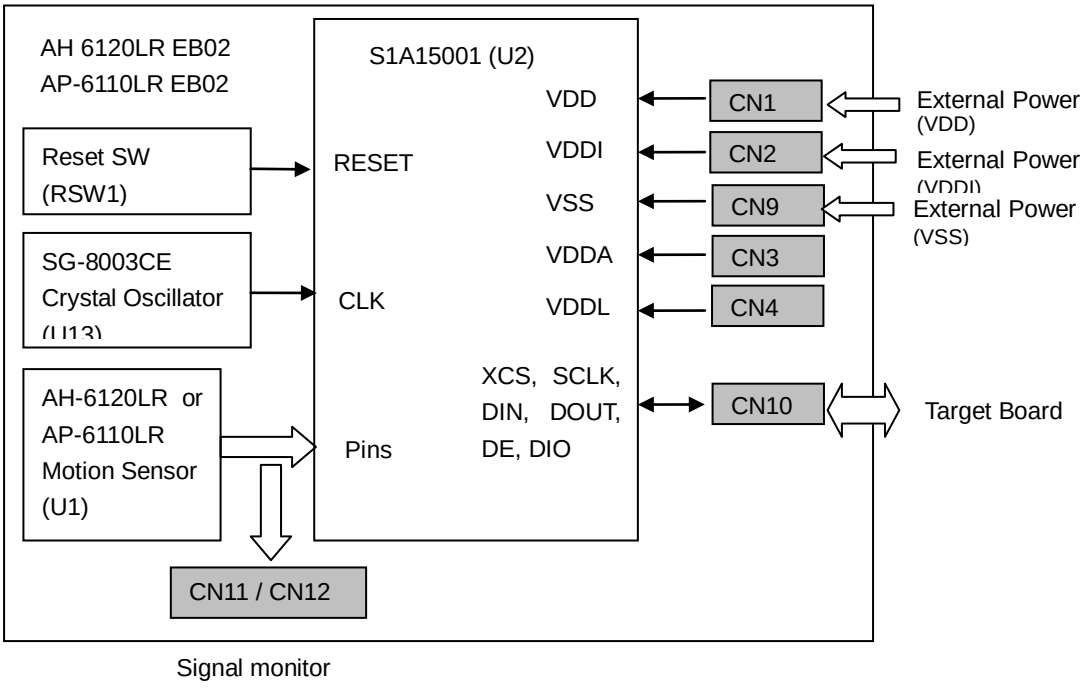


Fig. 2.1 Block Diagram

3. Hardware Information

3.1. Layout Information

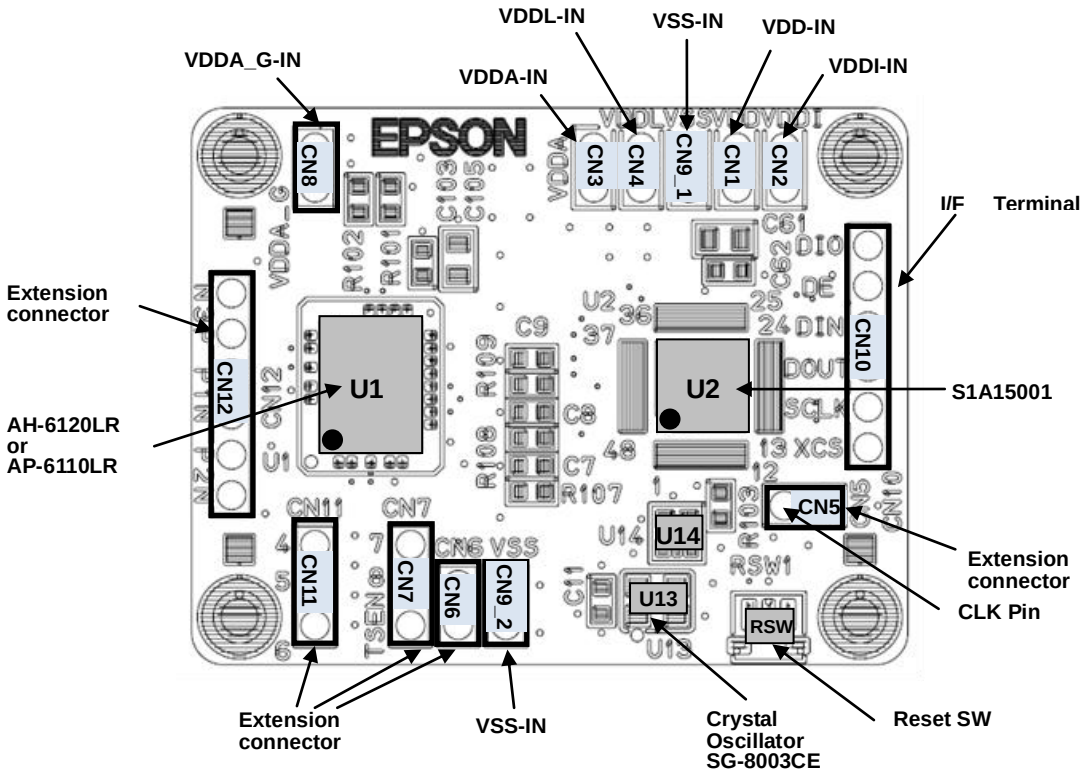


Fig. 3.1 Parts Layout (Surface)

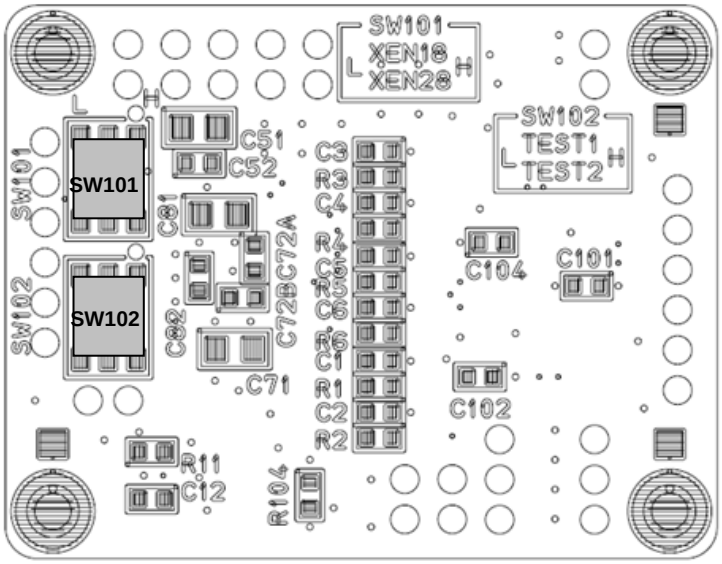


Fig. 3.2 Parts Layout (Back)

External dimension: 45 x 35 mm
Through-hole distance: 39 x 29 m

3.2. Outside dimension

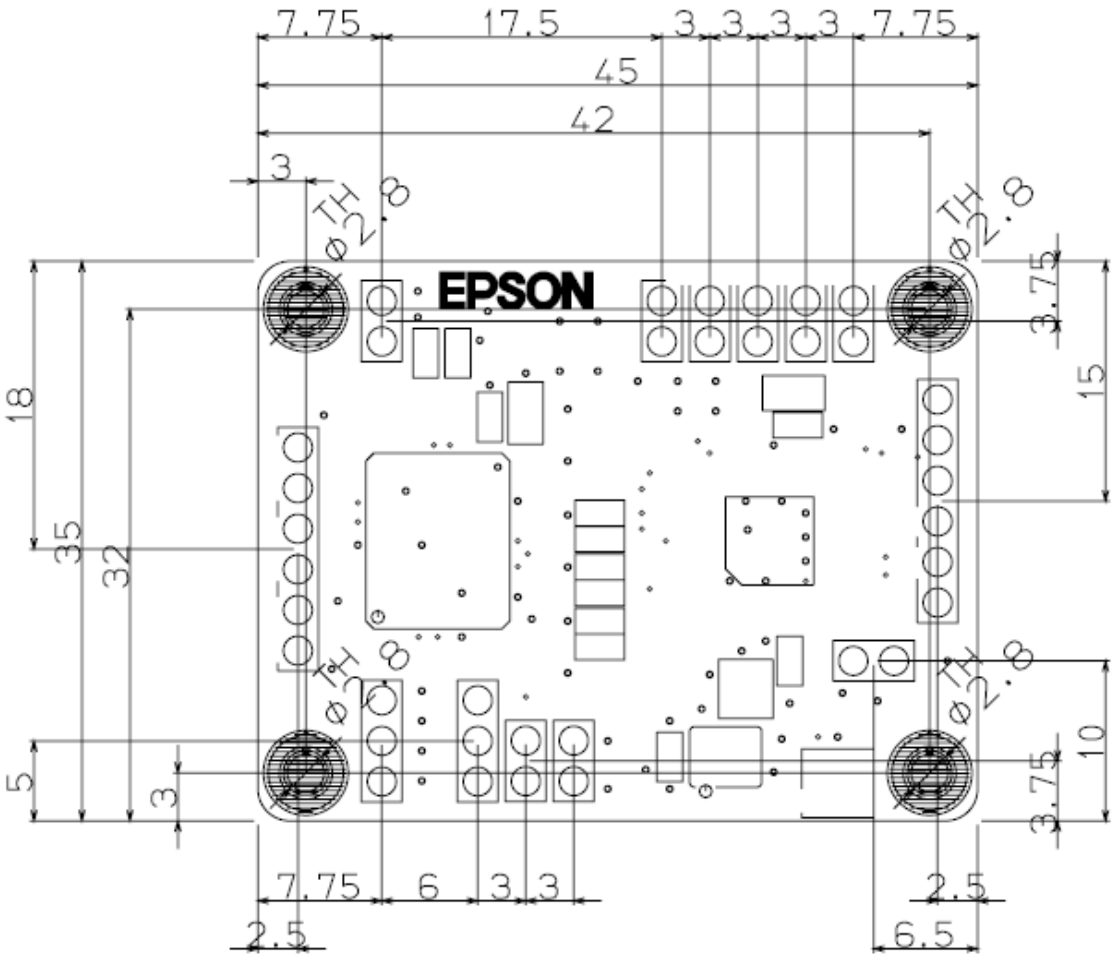


Fig. 3.3 Outside dimension (unit:mm)

3.3. SW Function

Table 3.1 SW Function

Location	Function
SW101 XEN18	VDDL regulator “L”: Enable “H”: Disable External Power
XEN28	VDDA regulator “L”: Enable “H”: Disable External Power
SW102 TEST1	Fixed: connect to “L”=VSS
TEST2	Fixed: connect to “L”=VSS

3.4. Connector pin assignment

Table 3.2 CN10 Connecter pin Assignment

Pin No	Name	Note
-	DIO	General I/O port
-	DE	Non-measuring (Before measurement start command input) Enable I/F signal acceptance condition “H” is reset released. Under measuring flag. (start to stop) Enable ADC data read. “H” is data updated.
-	DIN	Data input terminal
-	DOUT	Data output terminal All terminals disable when chip select is non-active
-	SCLK	Data transmitting clock input. Max:10MHz
-	XCS	Chip select terminal “L”: active. It’s possible data/command input “H”: non active

Table 3.3 CN11 Connecter pin Assignment

Pin No	Name	Note
4	VOAX	Accelerometer X monitor
5	VOAY	Accelerometer Y monitor
6	VOAZ	Accelerometer Z monitor

Table 3.4 CN12 Connecter pin Assignment

Pin No	Name	Note
2N	VREF_GY	Gyro sensor Vref Y monitor
P2	VOUT_GY	Gyro sensor Vout Y monitor
1N	VREF_GX	Gyro sensor Vref X monitor
P1	VOUT_GX	Gyro sensor Vout X monitor
P3	VOUT_GZ	Gyro sensor Vout Z monitor
N3	VREF_GZ	Gyro sensor Vref Z monitor

Table 3.5 CN5 Connecter pin Assignment

Pin No	Name	Note
-	CLK	Clock input(Please refer to Fig.3.1 Parts Layout(Surface))
-	VSS	GND

Table 3.6 CN6 Connecter pin Assignment

Pin No	Name	Note
-	ITRS	Test pin
-	ITRS	Test pin

Table 3.7 CN7 Connecter pin Assignment

Pin No	Name	Note
7	AIN7	Analog signal input
8	AIN8	Analog signal input
-	TSEN	Test pin

3.5. Circuit drawing

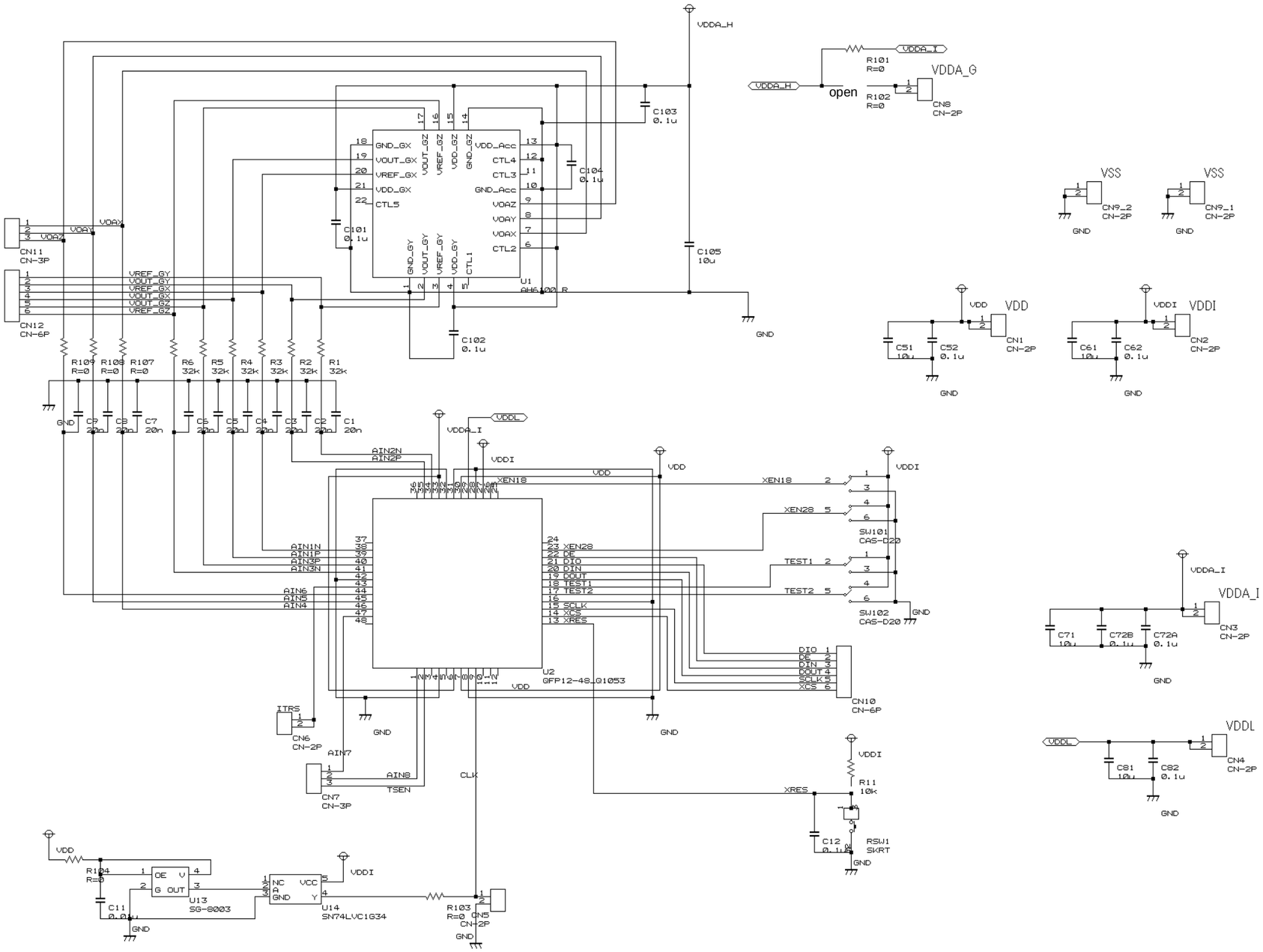


Fig3.4 AH-6120LR EB02 / AP-6110LR EB02 Circuit Drawing

3.6. Parts List

Table 3.8 AH-6120LR EB02 / AP-6110LR EB02 Parts List

Parts Name	Location	Spec	Number	Manufacture
Motion Sensor	U1	AH-6120LR / AP-6110LR	1	Seiko Epson
Analog front end IC	U2	S1A15001	1	Seiko Epson
Crystal Oscillator	U13	SG-8003CE	1	Seiko Epson
Universal Logic	U14	SN74LVC1G34DCKR	1	Texas Instruments
Tip Resistance	R11	MCR03EZPJ103 10k ohm	1	Rohm
Tip Resistance	R1,R2,R3,R4,R5,R6	MCR03EZPJ303 30k ohm	6	Rohm
Tip Resistance	R101,R103,R104, R107,R108,R109	RK73Z1ETTP 0 ohm	6	KOA
Ceramic Capacitor	C11	GRM188B11E103KA01D 0.01uF,25V+-10%	1	Murata
Ceramic Capacitor	C12,C52,C62,C72A, C72B,C82,C101, C102,C103,C104	GRM188B11E104KA01D 0.1uF,25V+-10%	10	Murata
Ceramic Capacitor	C51,C61,C71,C81, C105	GRM21BB31A106KE18 10uF,10V+-10%	5	Murata
Ceramic Capacitor	C1,C2,C3,C4,C5,C6 , C7,C8,C9	GRM188B11H223KA01D 22nF 16V+-10%	9	Murata
Switch	SW101,102	CAS-D20TB2	2	Copal.
Switch	RSW1	SKRTLBE010	1	Alps Electric
Connecter	CN1,CN2,CN3,CN4, CN5,CN6,CN8, CN9_1,CN9_2	WL-1(2pin)	9	Mac8
Connecter	CN7,CN11	WL-1(3pin)	2	Mac8
Connecter	CN10,CN12	WL-1(6pin)	2	Mac8

4. Typical operation

The operation of the EB02 board requires a compatible serial host interface connection through the appropriate pins on CN10. For full technical information on the interface please refer to the S1A15001 AFE IC Specification.

The following is a brief description of the typical operation and sequence to enable sampling of the U1 6DoF Motion Sensor. Please adjust the settings and configuration to suit your specific application.

4.1. Power Connection Settings

Connect the voltage supply to the EB02 board for system GND and voltage supply refer to Table 4.1.

Table 4.1 Typical Power Connection Settings

External	EB02 Board	Comment
	XEN28 = LOW	Use internal regulator controlled by REG_ON/REG_OFF command
	XEN18=LOW	Use internal regulator triggered by VDD power on
System GND	VSS	
System 3.3V	VDD and VDDI	VDDI is the interface voltage supply (from 1.65V to VDD). In this example, we assume the interface voltage is 3.3V

4.2. Host Serial Interface Settings

For more detailed information please refer to Section 6.1 and Section 11.2 of the S1A15001 AFE IC Specification.

- 8-bit SPI interface
- Polarity = 0, Phase = 0 (SCLK is idle LOW, data capture on rising edge)
- Connection through I/F Pin Terminal or CN1
- SCLK Frequency Max 10MHz

4.3. Example Sequence

The example sequence will configure the S1A15001 AFE IC with the following settings:

- 3-axis Gyro AIN1, AIN2, AIN3
- 3-axis Accelerometer AIN4, AIN5, AIN6
- Temp-Volt
- Sampling Rate = 2MHz/2048 = 977sps
- FIFO Setting = 1 Register/Channel
- Digital Filter = All channels 250Hz

The following is description of a typical sequence and serial communication for obtaining sensor data using the EB02 board.

1. The general sequence from power-on condition is to first issue a SOFTWARE RESET to place the S1A15001 U2 into a known state.
2. A short delay is required for reset recovery before any further commands are issued.
    a. The host should wait for atleast 3 CLK periods to guarantee 2 rising edge CLK cycle periods has taken place, or
    b. The host can sample the DE output pin for a “HIGH” state after issuing the SOFTWARE RESET command to determine when the reset is completed.
3. Send the MEASUREMENT SETTING to select which analog inputs will be enabled for sampling.
    a. For typical case, AIN1 ~ AIN6 is enabled for sampling of the 3-axis gyro and 3-axis accelerometer sensors, and Temp-Volt is enabled to sample the temperature.
4. Send the DIGITAL FILTER SETTING command to select the desired cutoff frequency of each analog input (250Hz, 125Hz or bypass).
5. Send the REG_ON which will turn on the internal voltage supply regulator for VDDA (which typical supplies power to the 6DoF sensor IC)
6. A minimum 500msec delay is required to allow the regulator supply to stabilize
7. Send the MEASUREMENT START to enable the internal sampling logic.

   The DE signal of that time goes LOW.
8. Wait for the DE signal to go HIGH.
9. Send READ DATA with the desired AINx channel in one CONTINUOUS DATA READ or individual READ DATA commands. This should be completed before the DE signal goes LOW.
10. To read another set of sensor data goto to step 8.
11. When sensor sampling is complete, send MEASUREMENT STOP to disable the internal sampling logic.
12. Send REG_OFF which will turn off the internal regulator supply VDDA to the 6DoF sensor.
13. Sequence Complete.

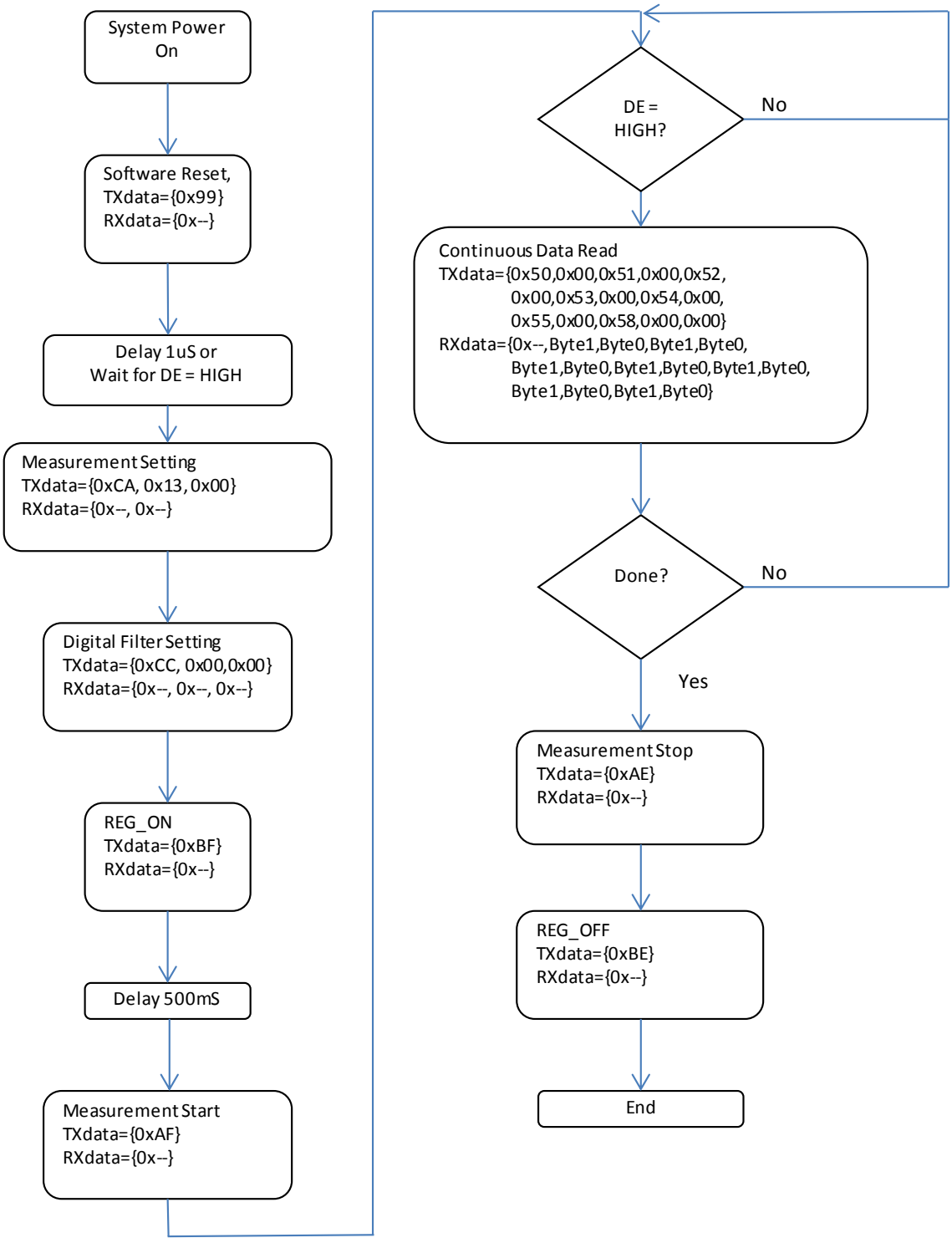


Fig. 4.1 Example Sequence Flow Diagram

Part 2 : Interface section

1. Outline

This product offers an optimum AFE (Analog Front End)-IC for motion sensing that transfers analog signals from a multi axis sensor into a digital signal to a CPU.

Analog signals from gyroscope and accelerometer will be converted to digital signal by an embedded 12-bit A/D converter.

Gyroscope signals are measured with high accuracy by the Out-Vref differential voltage measurement and removal of common mode voltage on the x, y, z for each axis.

The AFE IC provides a 1 chip solution for a high accuracy measurement circuit and reduce system component count for the addition of motion sensing function being easily added to an equipment.

2. Feature

- Embedded 8ch motion sensor measurement circuit (Gyro=3 channel , Accelerometer=3 channel)
  Gyro sensor input: Differential 3ch
  The Gyroscope signal is measured with high accuracy by Out-Vref differential voltage measurement.
  Available common “0 point voltage” of x, y, z each axis.
  Accelerometer input: Single input 3 channel
  Maximum input range: 0V to VDDA

- Embedded 12-bit SAR ADC
  ADC resolution: 12bits

- Sampling rate: 0.5~8kHz (at CLK=2.048MHz)

- Embedded digital filter: LPF (at sampling frequency fs = 1kHz)
  250Hz, 125Hz, or bypass

- Embedded voltage regulator for sensor drive / analog circuit
  VDDA=3.0V (VDD>=3.2V)
  VDDL=1.8V

- Embedded Temperature voltage circuit
  Scale Factor 3.6mV/℃

- System interface: SPI

- Voltage range: VDD-VSS = 3 to 3.6V (HISD：2.85 to 3.3V typ=3.0V)
- VDDA=2.85V to VDD
- VDDI=VDDL to VDD
- VDDL=1.65 to 1.95V

- Operating temperature range : -40 to +85°C

- Packaging style: PKG QFP12-48pin 9.00mm×9.00mm(body with pin)

3. Block diagram

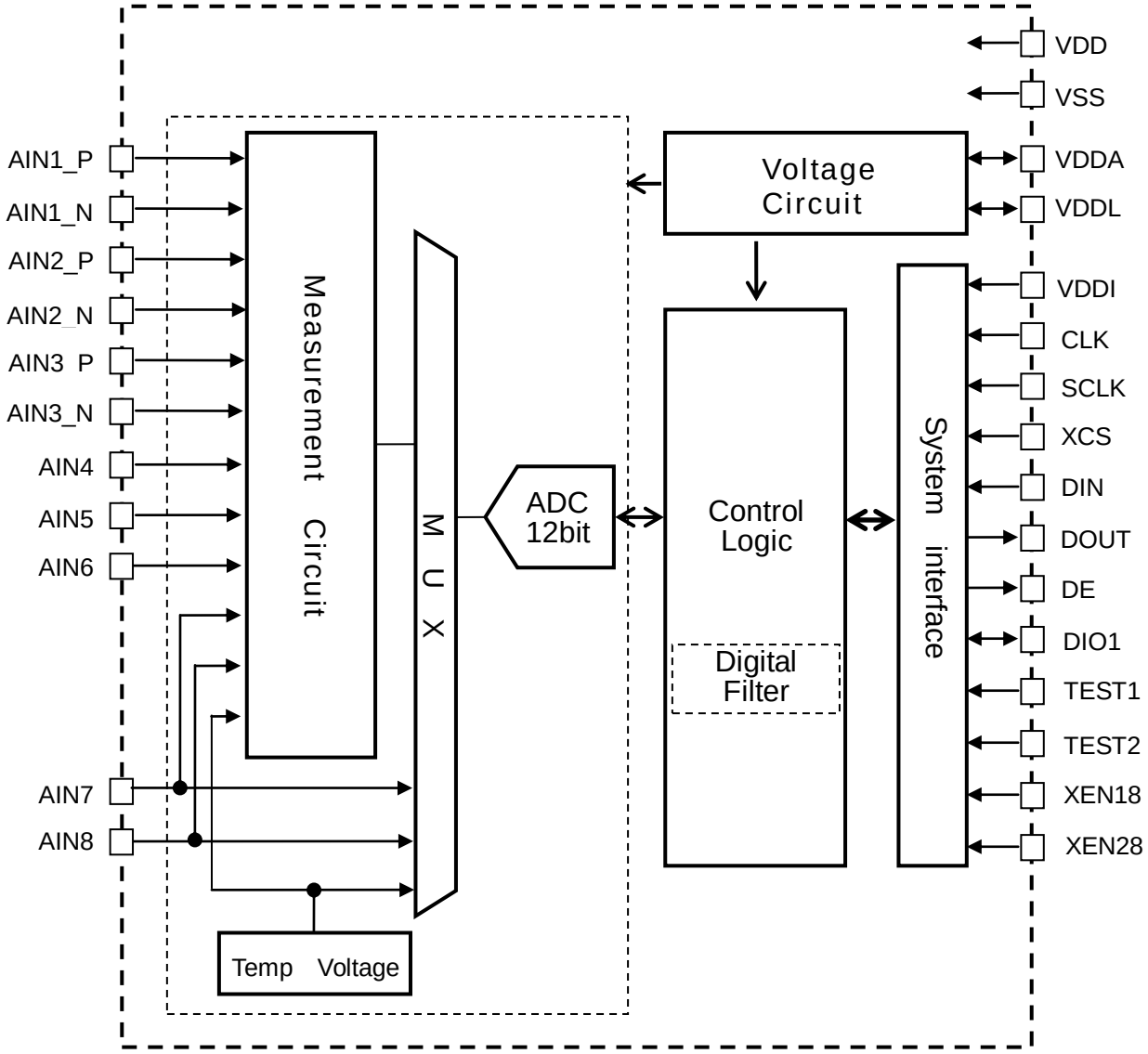


Fig 1 Block diagram

4. PKG Spec

4.1. QFP12-48PIN

QFP12-48PIN　7.00mm×7.00mm（body）、9.00mm×9.00mm（with Pin）、PINpitch：0.5mm

Top View

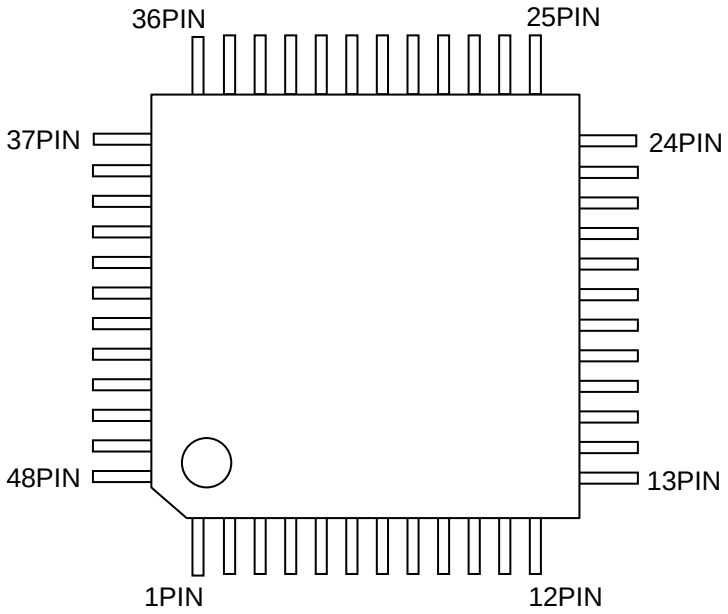


Fig 2　PKG　PIN　Layou

4.2. PKG　Pin　Layout（QFP12-48 Pin）

Table 1 PKG Pin Layout

PIN No	Pin Name	PIN No	Pin Name	PIN No	Pin Name	PIN No	Pin Name
1	AIN8	13	XRES	25	NC	37	NC
2	TSEN	14	XCS	26	XEN18	38	AIN1N
3	NC	15	SCLK	27	VDDI	39	AIN1P
4	VSS(A)	16	VSS	28	VSS(L)	40	AIN3P
5	NC	17	TEST2	29	VDDL	41	AIN3N
6	VDDA	18	TEST1	30	VDD	42	VSS(A)
7	VDD	19	DOUT	31	VSS	43	ITRS
8	VSS	20	DIN	32	VSS(A)	44	AIN6
9	CLK	21	DIO	33	VDDA	45	AIN5
10	NC	22	DE	34	AIN2N	46	AIN4
11	NC	23	XEN28	35	AIN2P	47	AIN7
12	NC	24	NC	36	NC	48	NC

5. Pin Map

5.1. Voltage Supply

Table 2 Voltage Supply

Name	I/O	Connect to	Note	Number of pins
VDD	Power	External power	Voltage supply Both of 2 VDD (Pin No.7,30) is not connected each in IC. Please connect supply each.	2
VSS VSS(A)	Power	External power	Ground terminal Connect to 0V (GND)	7
VDDA	Power	Capacitor	Sensor power / Analog circuit power	2
VDDL	Power	Capacitor	Internal logic power	1
VDDI	Power	External power	I/F power	1

5.2. Sensor Connection Pin

Table 3 Sensor Connection

Name	I/O	Connect to	Note	Number of pins
AIN1_P	I	G sensor	Gyro sensor out	1
AIN1_N	I	G sensor	Gyro sensor Vref out	1
AIN2_P	I	G sensor	Gyro sensor out	1
AIN2_N	I	G sensor	Gyro sensor Vref out	1
AIN3_P	I	G sensor	Gyro sensor out	1
AIN3_N	I	G sensor	Gyro sensor Vref out	1
AIN4	I	A sensor	Accelerometer out	1
AIN5	I	A sensor	Accelerometer out	1
AIN6	I	A sensor	Accelerometer out	1
AIN7	I	sensor	Sensor out	1
AIN8	I	sensor	Sensor out	1

5.3. Control Pin

Table 4 Control Pin

Name	I/O	Connect to	Note	Number of pins
XCS	I	MPU	Chip select terminal “L”: active. It’s possible data/command input “H”: non active	1
DIN	I	MPU	Data input terminal All terminals disable when chip select is non-active	1
DOUT	O	MPU	Data output terminal All terminals disable when chip select is non-active	1
SCLK	I	MPU	Data transmitting clock input. Max:10MHz	1
CLK	I	External clock	Clock input. 2.048MHz	1
DE	O	MPU	When sensor signal measurement is not active (Before measurement start command input) I/F signal is ready condition “H” is reset released. When sensor signal measurement is active.(measurement start to stop) Indicates that sensor ADC data read is ready condition. “H” is data updated and ready.	1
XRES	I	MPU	System reset “L”: active “H”:non active	1
DIO	I/O	–	General I/O port	1
XEN18	I	–	VDDL regulator “L”: Enable（=VSS） “H”: Disable（=VDDI）	1
XEN28	I	–	VDDA regulator “L”: Enable（=VSS） “H”: Disable（=VDDI）	1

5.4. Test pin

Table 5 test Pin

Name	I/O	Connect to	Note	Number of pins
TEST1	I	–	Test setting terminal Fixed “L”=VSS	1
TEST2	I	–	Test setting terminal Fixed “L”=VSS	1
ITRS	O	–	Test terminal Left open No connection	1
TSEN	O	–	Test terminal Left open No connection	1

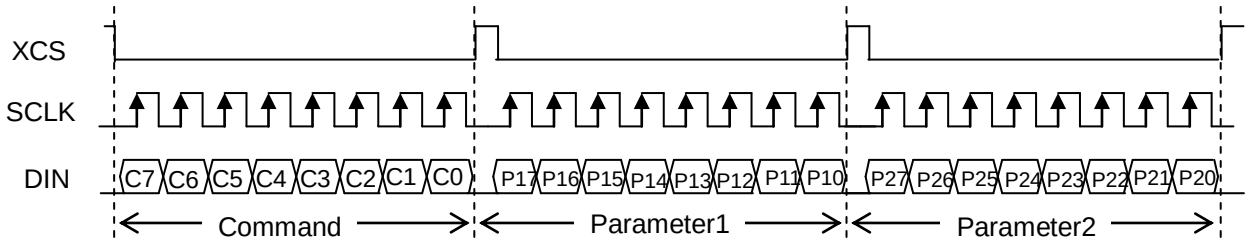
6. Function

6.1. System interface

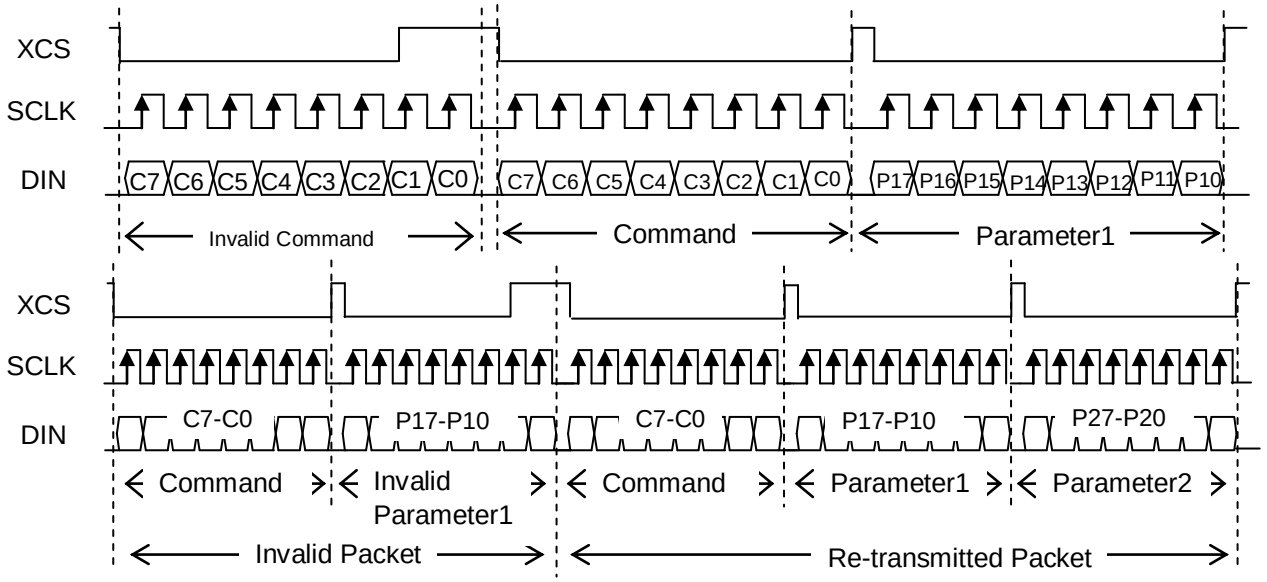
This IC communicates with the host MCU using a SPI serial bus interface.
This serial interface consists of four lines (chip selection (XCS), serial clock (SCLK), serial data input (DIN), and serial data output (DOUT)).
Data communication is enabled using an active LOW chip select (XCS="L").
The data transfer is done in eight bits. The host MCU inputs serial data sequentially and latched from MSB on the rising edge of the SCLK serial clock.
It is recommended that the XCS signal be set "H" every eight bits to prevent the malfunction by the noise. (The internal serial counter is reset at the time the XCS signal is driven HIGH.)
When D0 (or the 8th bit) is latched with the serial transfer clock SCLK, the byte is internally processed. Even if more data is driven on the serial interface than the required number of parameters defined by each command, it is invalid and ignored.

■Command Input

The XCS chip select must be set "L" while transmitting 1 byte of serial data (1Packet). The XCS chip select must be set “L” when SCLK is “L”.
It is necessary to keep XCS at “L” level while transmitting serial data (1packet). When set “H” at XCS during 1 packet transmitting , packet under transmitting is canceled. When “L” is set at XCS again, re-transmitting is enabled.



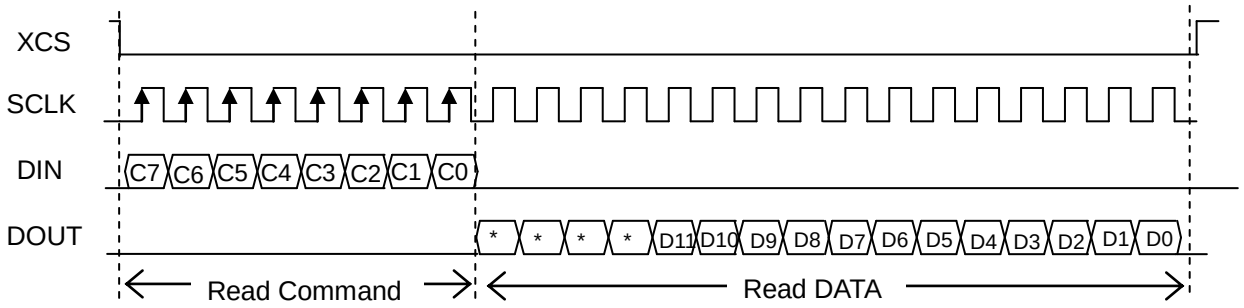
When XCS chip select is set “H” in the middle of a 1 byte serial data (1 packet), the current packet is canceled. When the XCS chip select is set “L” again, re-transmitting is enabled.



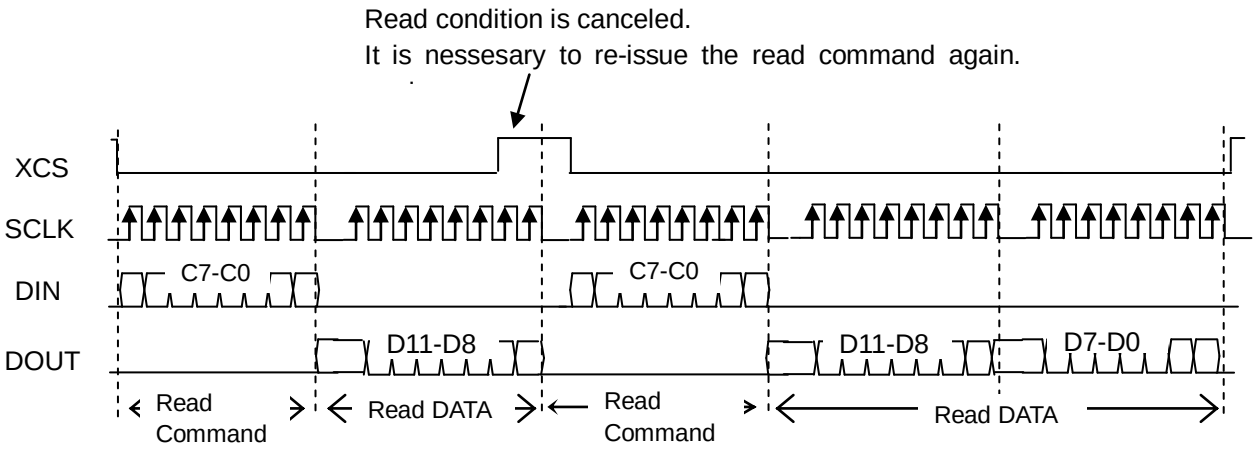
■Data Read

Please follow the below sequence for “Measurement data reading”. XCS must be set “L” when SCLK is “L” and the XCS must be hold “L” until data read is complete.

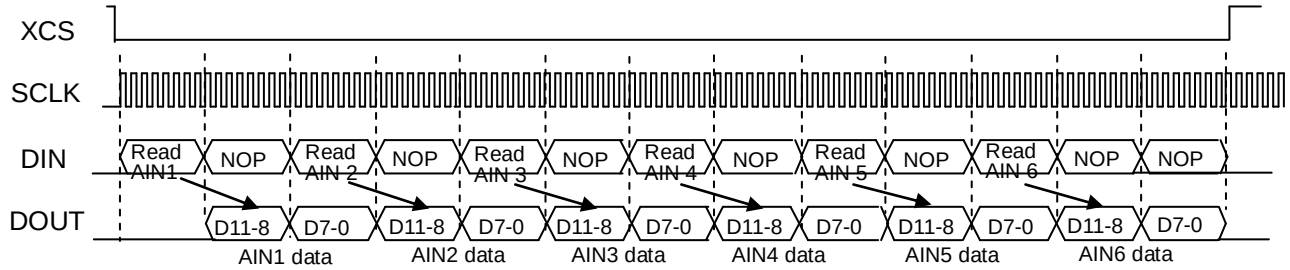
XCS must be set “H” after last bit is transmitted.



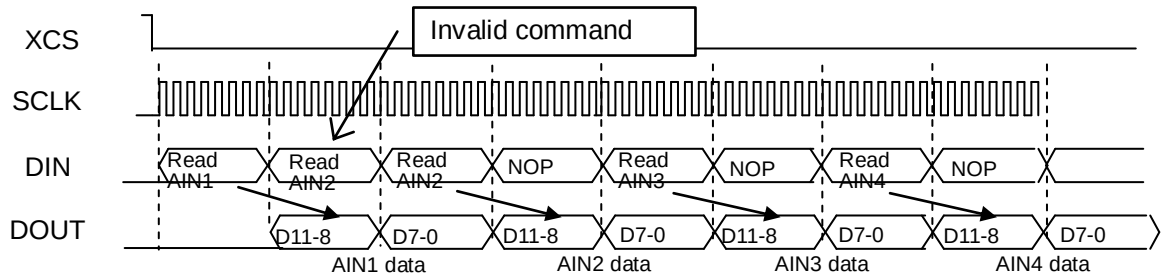
When XCS is set “H” during read data transmitting, the read condition is canceled. Set XCS “L” again, issue another command.



Continuous Data Read

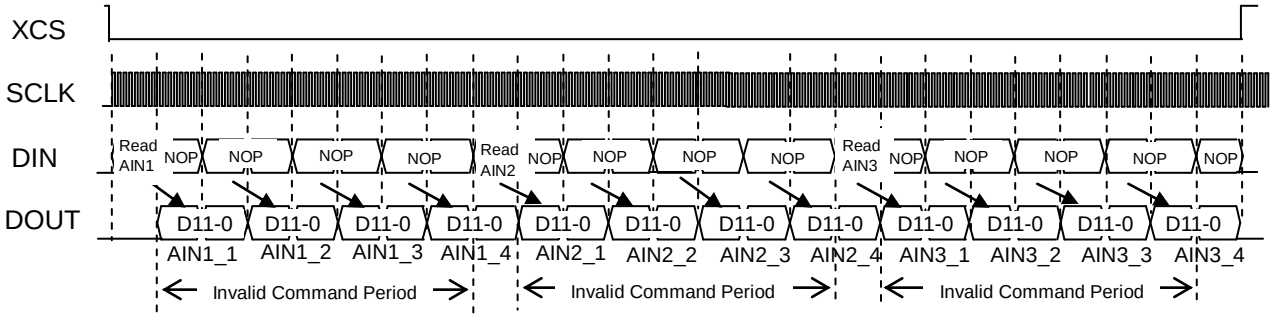


When a channel data read command is input during the expected NOP period, the command is invalid and ignored.



Data Read （FIFO 4register/ch setting）

It has the FIFO function（max:28registers）



6.2. Measurement Circuit

The measurement circuit of gyro sensor signal is output to ADC by mixed voltage with combined Out-Vref differential voltage and AGND (standard voltage).

AGND=1/2xVDDA

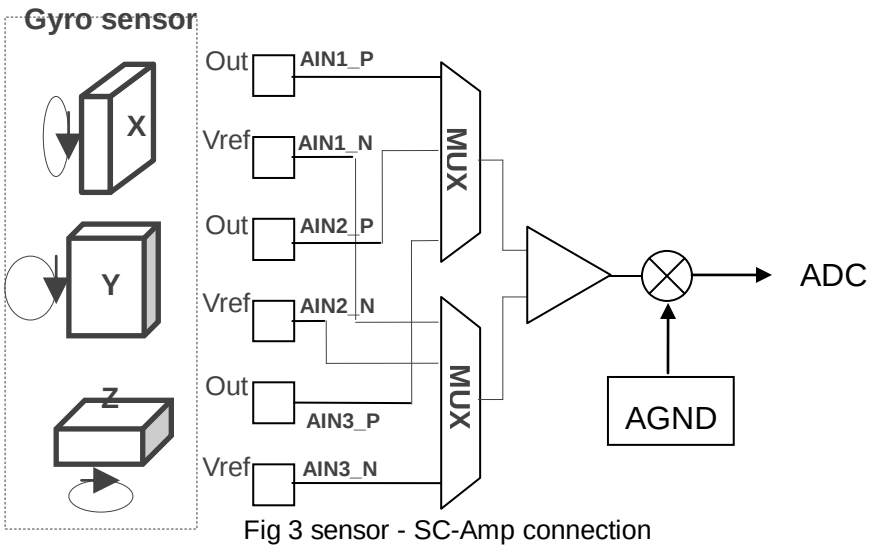
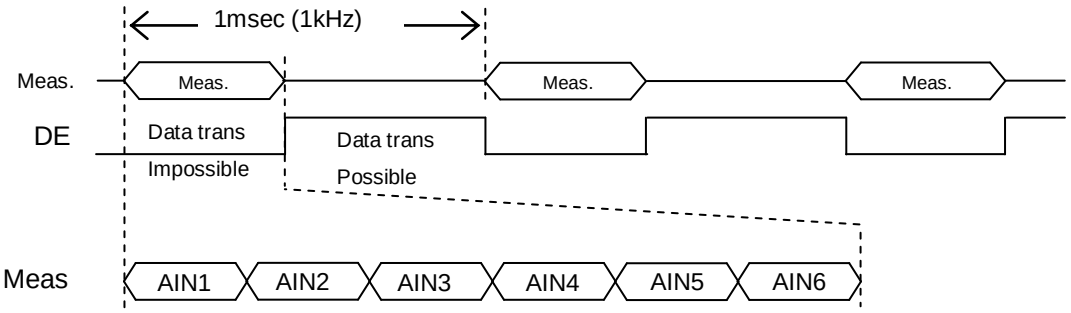
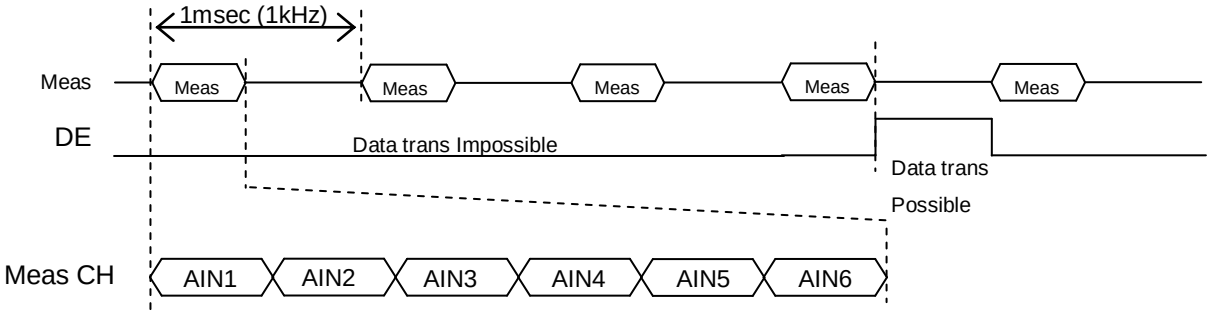


Fig 3 sensor - SC-Amp connection

Measurement timing



Measurement timing （As using FIFO 4Register/ch setting）



6.3. ADC circuit

Successive approximation type 12bitADC is embedded.
9ch multi input compliant.
Measurement channel sequence is
AIN1→AIN2→AIN3→AIN4→AIN5→AIN6→AIN7→AIN8→Temp-Volt.
If measurement channel is disabled (command: CAh) the channel is skipped.

6.4. Digital filter

Internal digital filter.
Separate cut off frequency setting is available for channel AIN1-3,AIN4-6,AIN7,AIN8,and Temp-Volt.
Cut off frequency is selectable 250Hz, 125Hz, bypass. (Sampling frequency fs=1 kHz)

6.5. Power supply and configration control option

Embedded 3 voltage regulators as below.
VDDA: Supply 3.0V for measurement circuit and sensors.
AGND: Supply standard voltage (VDDA/2) for measurement circuit.
VDDL: Supply 1.8V for internal logic.

6.5.1.VDDA regulator

Operated by control terminal (XEN28) and command.
XEN28="L": Using internal regulator
ON/OFF controlled by command.
XEN28="H": Using externally supplied VDDA
Control is not possible by command.
Output is fixed 3.0V+/-10mV by before shipment from plant.

6.5.2.AGND regulator

ON/OFF controlled by command.
VDDA/2 is out on AGND.

6.5.3.VDDL regulator

Operated by control terminal (XEN18).
XEN18="L": Using Internal regulator.
Regulator is triggered by VDD power on.
XEN18="H": Using externally supplied voltage regulator.

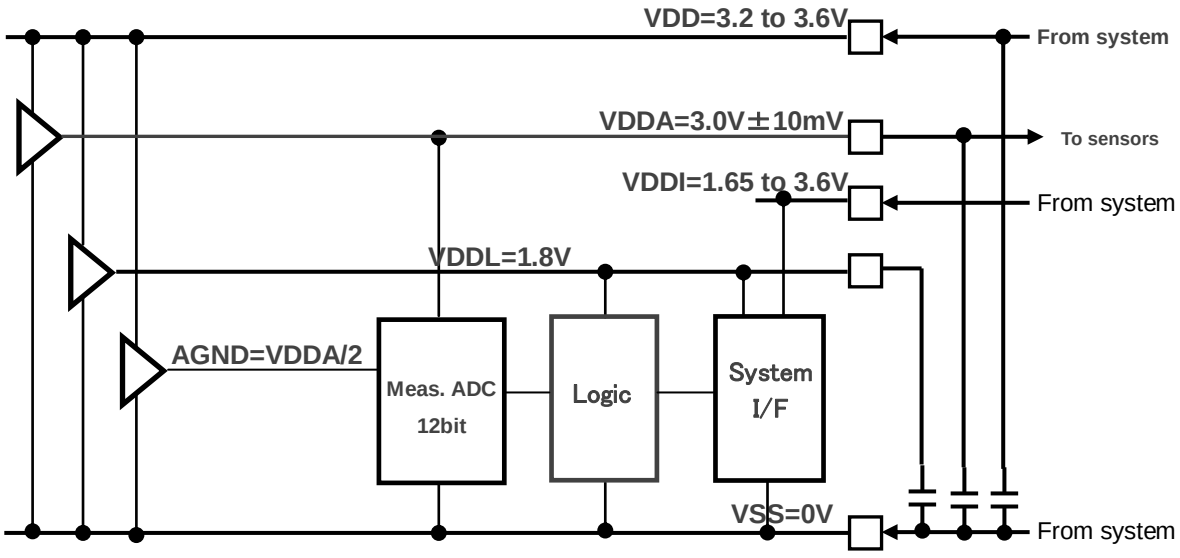
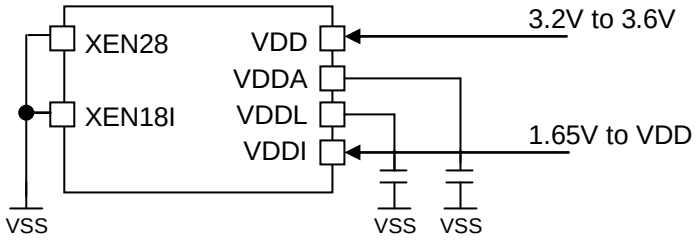


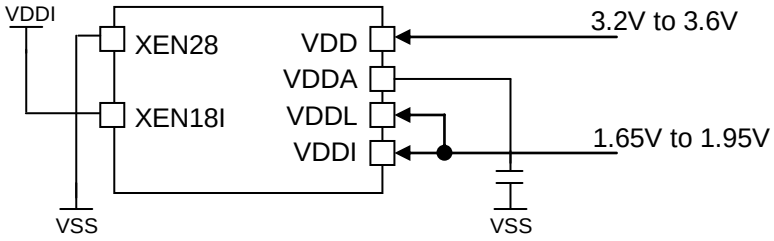
Fig4 Power supply block diagram

6.6. Power supply and connection example options

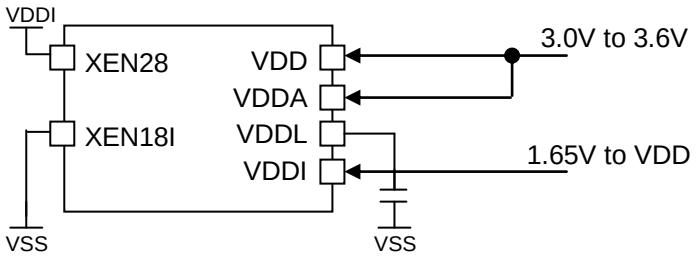
(1) Single power input XEN18="L"、XEN28="L"
I/F power with MCU: Externally supplied.
Analog power: VDDA control from internal regulator.
Internal logic power: VDDL control from internal regulator.



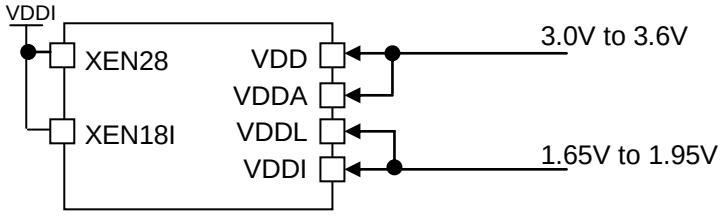
(2) Dual power input XEN18="H"、XEN28="L"
I/F power with MCU: Externally supplied with VDDI=VDDL.
Analog power: VDDA control from internal regulator.
Internal logic power: Externally supplied with VDDL=VDDI.Internal regulator is disabled.



(3) Single power input XEN18="L"、XEN28="H"
I/F power with MCU: Externally supplied.
Analog power: Externally supplied with VDDA=VDD.Internal regulator is disabled.
Internal logic power: VDDL control from internal regulator.



(4) Dual power input XEN18="H"、XEN28="H"
I/F power with MCU: Externally supplied with VDDI=VDDL.
Analog power: Externally supplied with VDDA=VDD.Internal regulator is disabled.
Internal logic power: Externally supplied with VDDL=VDDI.Internal regulator is disabled.



6.7. Reset circuit

Digital circuit is reset by “Power on reset”,”External in: XRES”, or “Software reset command”. Initialization by asserting XRES during power on is recommended. After reset by XRES, each terminal should be under normal control. Pulse width of reset “L” must be longer than 20nsec.

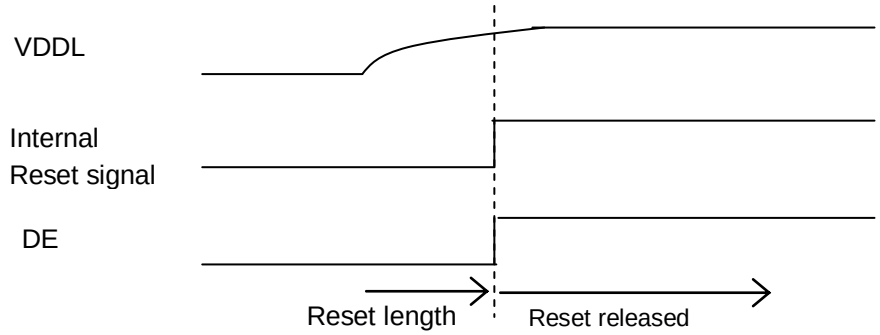
Initialization reset timing is shown by below for “Power on reset”,”External in: XRES”, “Software reset command”.

6.7.1. Power on and circuit initialization timing

Power on reset

Power on signal is generated by monitoring the internal logic power supply VDDL.

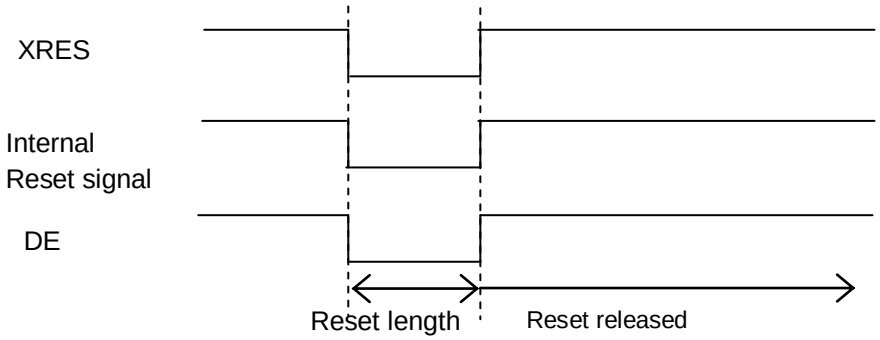
Power on reset timing



6.7.2. External reset control (XRES=H->L->H)

Manual asynchronous hardware reset available by a level sensitive external XRES input pin (no relation with clock.

External reset timing



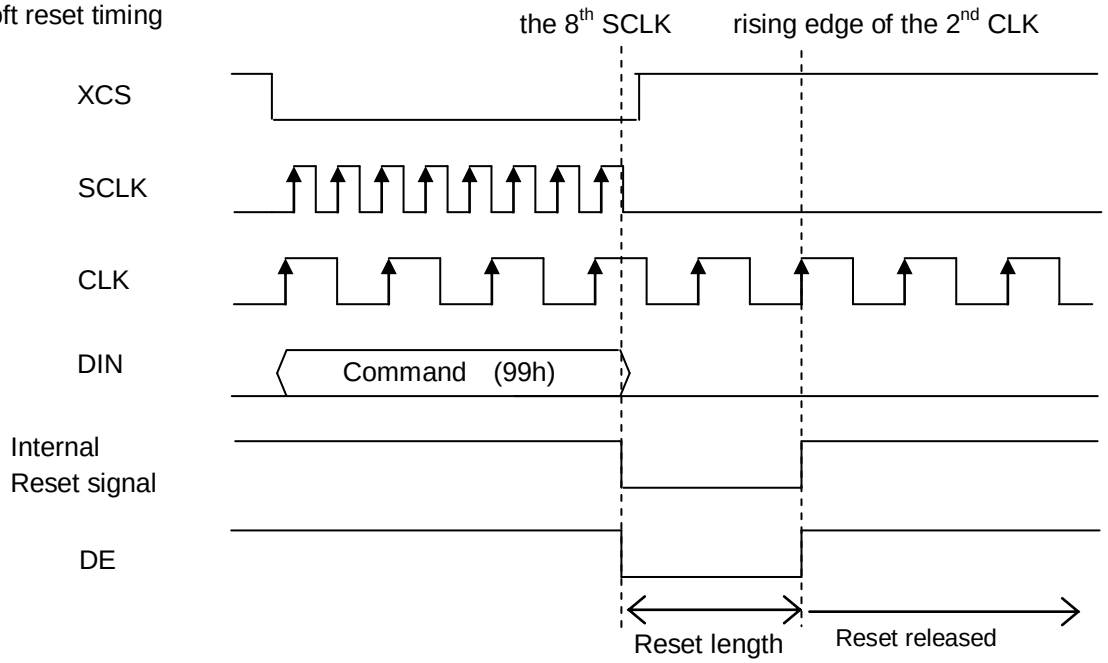
6.7.3. Software reset

The software reset by command interface is available.

The reset length is from the software reset command input (the 8th SCLK) to rising edge of (the 2nd CLK).

During this reset period, any command input from the serial interface is not accessible.

Soft reset timing



7. Command

There are two types of command. 1): Multi byte command with parameters. 2): 1 byte command without parameters. The interpretation and execution of command is done without external clock. The command and the parameter are defined by one bytes lengths (eight bits).

Do not use other command codes that are not on the command table as below.

7.1. Command table

No.	Command name	Command code (Hex)	Instruction length (Byte)	Command Execution timing	Function
1	Start measurement	AF	1	immediately after command issue	Start measurement
2	Stop measurement	AE	1	immediately after command issue	Stop measurement
3	REG_ON	BF	1	immediately after command issue	Internal regulator(VDDA)on
4	REG_OFF	BE	1	immediately after command issue	Internal regulator(VDDA)off
5	Measurement setting	CA	3	Measuring time	Measurement setting
6	Digital filter setting	CC	3	Measuring time	Digital filter setting
7	Read data	5 -	1	immediately after command issue	Read data
8	General port setting	D5	2	immediately after command issue	General port setting
9	Software reset	99	1	immediately after command issue	Software reset
10	NOP	00	1	—	Command that does no operation

7.2. Parameter default table

No.	Command	Parameter	Code (bin)								Hex	Default condition
			D7	D6	D5	D4	D3	D2	D1	D0		
5	Measurement setting	P1	1	1	1	0	0	0	0	0	E0	No measure channel
		P2	*	*	0	0	0	0	0	0	00	1kHz Sampling
6	Digital filter setting	P1	0	0	0	0	0	0	0	0	00	Digital filter 250Hz
		P2	*	*	*	*	*	*	0	0	00	Digital filter 250Hz
8	General port	P1	*	*	*	*	*	*	*	0	00	General port “L”out

7.3. Command function

7.3.1. Measurement start (command: AFh parameter: NONE)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	0	1	0	1	1	1	1	AF	Command measurement start

Begins measuring the sensor signal based on the measurement settings command and digital filter settings. The REG_ON command should be issued before issuing the measurement start command.

7,3,2, Measurement stop (command: AEh parameter: NONE)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	0	1	0	1	1	1	0	AE	Command measurement stop

Stops the sensor signal measurement. The measurement is stopped immediately after the command is accepted.

7.3.3. REG_ON (command: BFh parameter: NONE)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	0	1	1	1	1	1	1	BF	Command regulator activation

The internal power supply (VDDA, AGND) is started. A delay of 500 msec or more is recommended after entering the REG_ON command for the power supply circuits to stabilize before issuing a measurement start command.
In case of XEN28 ="H" (VDDA is externally supplied), only the AGND of the internal power supply is started by the REG_ON command.

7.3.4. REG_OFF (command: BEh parameter: NONE)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	0	1	1	1	1	1	0	BE	Command regulator stop

The internal power supply (VDDA, AGND) is stopped.

7.3.5. Measurement setting (command: CAh parameter: 2)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	1	0	0	1	0	1	0	CA	Command measurement channel setting
P17	P16	P15	P14	P13	P12	P11	P10	—	Parameter 1 measurement channel set
P27	P26	P25	P24	P23	P22	P21	P20	—	Parameter 2 measurement timing set

Parameter 1 measurement channel set

"1": Measurement
"0": Non measurement
P10: AIN1, AIN2, AIN3 (Gyro sensor)
P11: AIN4, AIN5, AIN6 (Accelerometer)
P12:AIN7
P13:AIN8
P14:Temp-Volt

Measurement circuit set
"1":Buff input
"0":ADC direct input
P15:AIN7
P16:AIN8
P17:Temp-Volt

Please setting P15-17 when use Buff.

Set value	P15	P16	P17
AIN7 use Buff	1	0	0
AIN7,AIN8 use Buff	1	1	0
AIN7,AIN8,Temp-Volt use Buff	1	1	1
AIN7,AIN8,Temp-Volt no use Buff	0	0	0

Parameter 2 measurement Sampling timing set

The measurement cycle (sampling rate) is decided by external clock (CLK) .
P22-20：measurement cycle set

P22	P21	P20	Set valu	Reference value CLK=2048KHz
0	0	0	CLK Clock frequency /2048(Hz)	1ksps
0	0	1	CLK Clock frequency /1024(Hz)	2ksps
0	1	0	CLK Clock frequency /4096(Hz)	500sps
0	1	1	CLK Clock frequency /512(Hz)	4ksps
1	0	0	CLK Clock frequency /256(Hz)	8ksps

The setting not described is prohibited.

P25-23 : FIFO Data Register set（Number of registers for each CH）
FIFO has 28 register max. Therefore, when AIN1-7 is measured, the maximum supported is four registers/CH P22-20=[010] .

P25	P24	P23	Set value
0	0	0	1 registers/CH
0	0	1	2 registers/CH
0	1	0	4 registers/CH
0	1	1	6 registers/CH
1	0	0	8 registers/CH
1	0	1	10 registers/CH
1	1	0	12 registers/CH
1	1	1	16 registers/CH

7.3.6. Digital filter setting (command: CCh parameter: 2)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	1	0	0	1	1	0	0	CC	Command digital filter setting
P17	P16	P15	P14	P13	P12	P11	P10		Parameter 1 cut off frequency set
*	*	*	*	*	*	P21	P20	—	Parameter 2 cut off frequency set

Internal digital filter is set.
The digital filter setting command is only valid while the measurement is stopped and the digital filter setting command is ignored if sent while measurement is already started. When changing the digital filter setting is required after measurement has started, issue the measurement stop command and input of the new digital filter setting command and the parameters is needed.

P11 P13 P15 P17 P21	P10 P12 P14 P16 P20	Cut off frequency
0	0	250Hz
0	1	125Hz
1	0	Setting prohibited
1	1	Through

P11, P10:AIN1 to 3 (Gyro sensor) input digital filter
P13, P12:AIN4 to 6 (Accelerometer) input digital filter
P15,P14 :AIN7 input digital filter
P17,P16 :AIN8 input digital filter
P21,P20 :Temp-Volt input digital filter

7.3.7. Read data (command: 5-h Read Data: 2)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	1	0	1	P13	P12	P11	P10	5—	Command read data
0	0	0	0	D11	D10	D9	D8	—	Read Data 1 upper 4bit
D7	D6	D5	D4	D3	D2	D1	D0	—	Read Data 2 lower 8bit

D7-D4: read command

P13-P10: read channel setting

P13	P12	P11	P10	Selected channel
0	0	0	0	AIN1
0	0	0	1	AIN2
0	0	1	0	AIN3
0	0	1	1	AIN4
0	1	0	0	AIN5
0	1	0	1	AIN6
0	1	1	0	AIN7
0	1	1	1	AIN8
1	0	0	0	Temp-Volt
1	0	0	1	Setting prohibited
1	0	1	0	Setting prohibited
1	0	1	1	Setting prohibited
1	1	0	0	Setting prohibited
1	1	0	1	Setting prohibited
1	1	1	0	Setting prohibited
1	1	1	1	Setting prohibited

Read data 0x00 is output for the below cases.

1) When specifying a AIN* channel that is not enabled by the measurement setting command.
2) When specifying and invalid AIN* channel setting parameter.

7.3.8. General port setting (command: D5h parameter: 1)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	1	0	1	0	1	0	1	D5	Command general port setting
*	*	*	*	*	*	*	P0	—	Parameter DIO data set

P0: set output value of general DIO.

P0=1: out”H” level.

P0=0: out”L” level.

7.3.9. Software reset (command: 99h parameter: NONE)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	0	0	1	1	0	0	1	99	Command Software reset

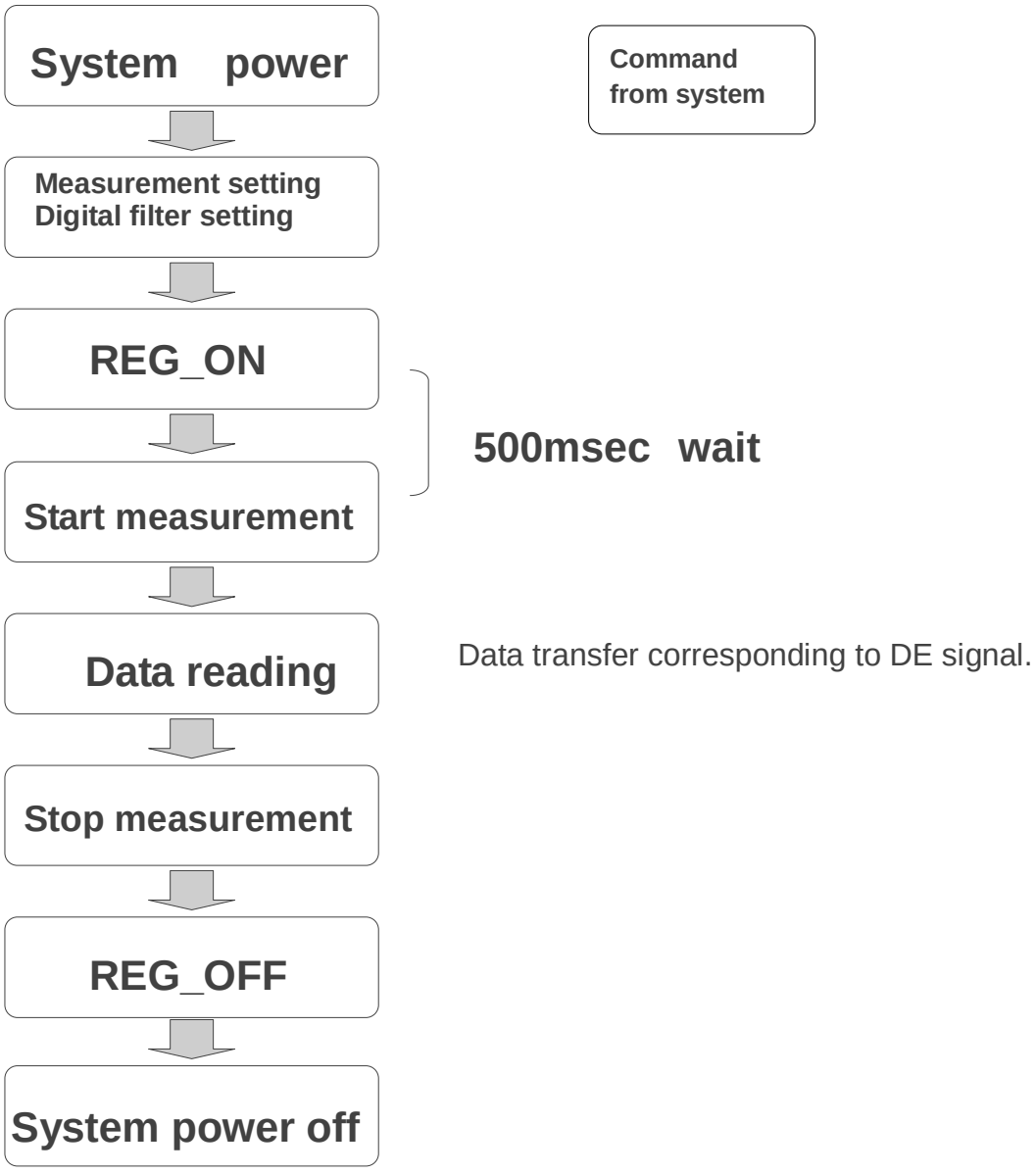
The software reset has similar effects to a hard reset.

7.3.10. NOP (command: 00h parameter: NONE)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	0	0	0	0	0	0	0	00h	Command Non Operation

The command for “No Operation” has no effect on chip operation.

Power on sequence



8. Absolute maximum ratings

Table 6 absolute maximum ratings

item	code	rating	unit
Supply voltage(1)	VDD	-0.3 to 5.5	V
Supply voltage(2)	VDDA	-0.3 to 5.5	
Supply voltage(3)	VDDL	-0.3 to 2.5	
Supply voltage(4)	VDDI	-0.3 to 5.5	
Supply voltage(5)	VSS	0.0	
Logic input voltage	VLIN	-0.3 to VDD + 0.3	V
Logic output voltage	VLOUT	-0.3 to VDD + 0.3	V
Operating temperature	ToPN	-40 to 85	°C
Storage temperature	Tstg	-55 to 125	

Note *1: All standard voltage is VSS = 0 V without notice.
*2: Based electric potential is VSS.
*3: When using over the range of stated above, IC might be destroyed. In additon it might influence the reliability of the IC if it uses it for a long time in the state of the absolute maximum rating.
*4: Please supply the voltage to become VDD>VDDA.

9. Recommended operation conditions

Table 7 recommended conditions (VDDI≠VDDL, VDDL: using internal regulator)

item	code	Operating voltage	unit
Supply voltage(1)	VDD	3.0 to 3.6	V
Supply voltage(2)	VDDA	2.85 to VDD	
Supply voltage(3)	VDDL	1.65 to 1.95	
Supply voltage(4)	VDDI	1.65 to VDD	
Supply voltage(5)	VSS	0.0	

Table 8 recommended conditions (VDDI=VDDL, VDDL: using external input)

item	code	Operating voltage	unit
Supply voltage(1)	VDD	3.0 to 3.6	V
Supply voltage(2)	VDDA	2.85 to VDD	
Supply voltage(3)	VDDL	1.65 to 1.95	
Supply voltage(4)	VDDI	1.65 to 1.95	
Supply voltage(5)	VSS	0.0	

Note *1: The operation of IC is guaranteed within the range of recommended operation condition.
*2: Please insert the bypass capacitor for the noise reduction near the power supply terminal.
*3: Operation is not guaranteed if operative with a rapid supply voltage change.
*4: Please supply the voltage such that VDD>=VDDA and VDD>=VDDI>=VDDL.

10. DC characteristics

Table 9 DC characteristics

VSS = 0 V, VDDI = 1.65 to 3.6V, VDDL = 1.65 to 1.95V, VDD = 3.0 to 3.6 V, Ta = -40 to 85ºC

item	code	conditions	rating			unit	terminal
			Min.	Typ.	Max.		
"L"input voltage	V_{IL}	–	V_{SS}	–	0.2 × V_{DDI}	V	Logic input
"H"input voltage	V_{IH}		0.8 × V_{DDI}	–	V_{DDI}		
Input leakage current	I_{LI}	V_{IN} = V_{DDI} or V_{SS}	-2.0	–	2.0	µA	Logic input
Analog leakage current	ILA	VDDA=3.6V VIN=VDDA or VSS	-4.8	–	4.8	µA	Analog input
Output leakage current	I_{LO}	V_{IN} = V_{DDI} or V_{SS}	-2.0	–	2.0	µA	Logic input
In/out leakage current	I_{LIO}	V_{IN} = V_{DDI} or V_{SS}	-2.0	–	2.0	µA	Logic input
Input capacitance	C_{IN}	Ta = 25 °C, f=1 MHz	–	–	25	pF	Logic input Analog input
"L"out voltage	V_{OL}	V_{DD} = 1.8 V I_{OL} = 0.06 mA I_{OH} = -0.06 mA	V_{SS}	–	V_{SS} + 0.3	V	Logic in/out-put
"H"out voltage	V_{OH}		V_{DDI} - 0.3	–	V_{DDI}		
Static current consumption	I_{DDIQ}	V_{DDI} = V_{DDL} = 1.8 V V_{DD} =V_{DDA}= 3.0 V	–	–	5.0	µA	V_{DDI}
	I_{DDLQ}		–	–	20.0	µA	V_{DDL}
	I_{DDAQ}		–	–	5.0	µA	V_{DDA}
	I_{DDQ}		–	–	5.0	µA	V_{DD}
Active current consumption 1	I_{DDI}	V_{DDI} = 1.8 V V_{DD} = 3.3 V VDDA,VDDL using Internal Regulater CLK=2MHz 7ch measurement 976.6sps	–	–	10	µA	V_{DDI}
	I_{DD}		–	202 *1	300	µA	V_{DD}
Active current consumption 2	I_{DDA}	V_{DDI} = 1.8 V V_{DD} = 3.3 V Externally supplied with VDDA,VDDL VDDA=3.0V VDDL=1.8V CLK=2MHz 7ch measurement 976.6sps	–	41 *1	60	µA	V_{DDA}
	I_{DDL}		–	105 *1	150	µA	V_{DDL}

*1 Ta=25 ºC

ADC

Table 10 ADC characteristics

VSS = 0 V, VDDI = 1.65 to 3.6V, VDDL = 1.65 to 1.95V, VDD = 3.0 to 3.6 V, Ta = -40 to 85 ºC

item	code	conditions	rating			unit
			Min.	Typ.	Max.	
Integral nonlinearity	INL	CLK=2.048MHz	-3		3	LSB
Differential nonlinearity	DNL	CLK=2.048MHz	-3		3	LSB
Full scale error	FSE	CLK=2.048MHz	-8.0		8.0	mV
Zero scale error	ZSE	CLK=2.048MHz	-8.0		8.0	mV

Internal Regulater circuit

Table 11 Constant voltage circuit characteristics

VSS = 0 V, VDDI = 1.65 to 3.6V, VDDL = 1.65 to 1.95V, VDD = 3.2 to 3.6 V, Ta = -40 to 85 ºC

item	code	conditions	rating			unit
			Min.	Typ.	Max.	
Output voltage (VDDL)	VDDL		1.7	1.8	1.9	V
Output voltage (VDDA)	VDDA	Ta=25 ºC、VDD=3.3V	2.990	3.0	3.010	V

Temp-Voltage Circuit

Table 12 Constant voltage circuit characteristics

VSS = 0 V, VDDI = 1.65 to 3.6V, VDDL = 1.65 to 1.95V, VDD = 3.0 to 3.6 V, Ta = -40 to 85 ºC

item	code	conditions	rating			unit
			Min.	Typ.	Max.	
Output voltage	Vtemp	Ta=25℃ VDDA=3.0V	1393	1477	1589	Code
Scale Factor	dVtemp	VDDA=3.0V	4.084	4. 800	5.515	code/℃

11. AC characteristics

11.1. Oscillating frequency

The external clock input frequency timing requirements are described below for the CLK pin terminal.

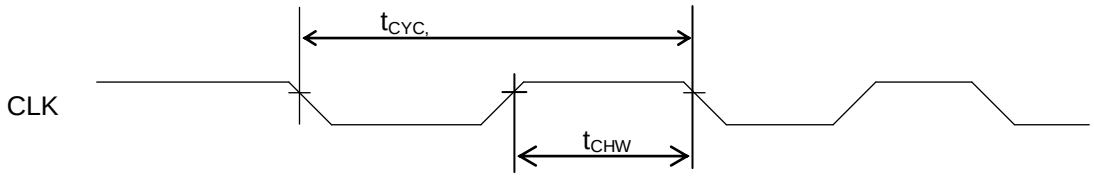


Fig 5 external clock in

Table 13 External clock in characteristics

VSS = 0 V, VDDI = 1.65 to 3.6V, VDDL = 1.65 to 1.95V, VDD = 3.0 to 3.6 V, Ta = -40 to 85 ºC

item	code	conditions	rating			unit
			Min.	Typ.	Max.	
External clock input frequency	1/tCYC		—	—	2.048	MHz
External clock input period	tCYC		0.488	—	—	usec
CLK duty	tCD	t_{CHW}/t_{CYC}	40	—	60	%

*1: All timing is provided for based on 20% and 80% of VDD.
*2: rise time (tr) and fall time (tf) is defined max.10 ns.

11.2. Serial interface (default : DOUT hold mode)

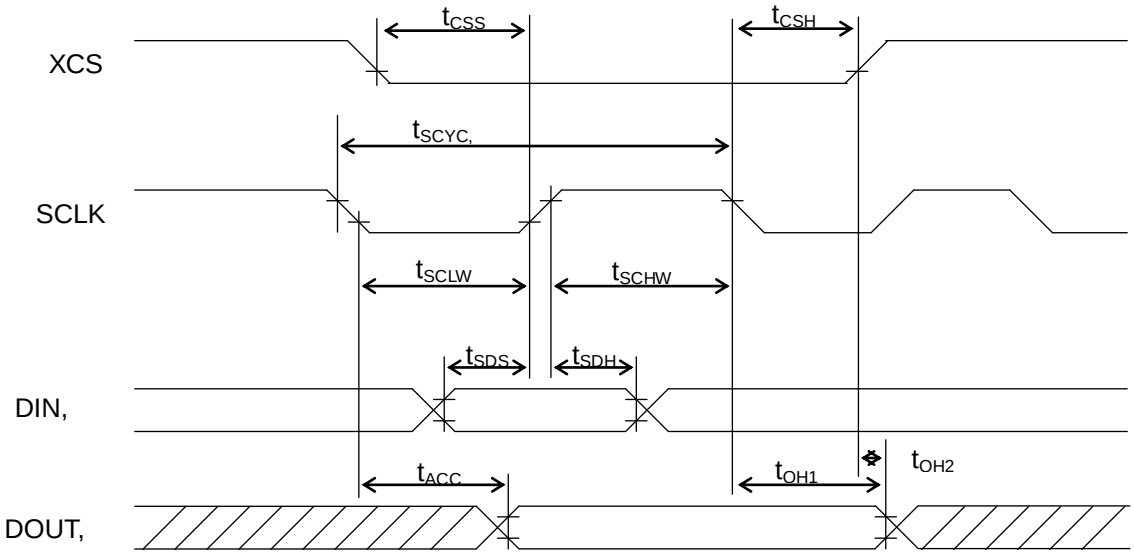


Fig 6 serial interface

Table 14 serial interface characteristics

VSS = 0 V, VDDI = 1.65 to 3.6V, VDDL = 1.65 to 1.95V, VDD = 3.0 to 3.6 V, Ta = -40 to 85 ºC

item	code	conditions	Min.	Max.	unit
SCLK period	tSCYC	–	100	–	ns
SCLK low level pulse width	tSCLW	–	40	–	
SCLK high level pulse width	tSCHW	–	40	–	
XCS set up time	tCSS	–	30	tSCCL	
XCS hold time	tCSH	–	30	tSCCL	
Data set up time	tSDS	–	10	–	
Data hold time	tSDH	–	10	–	
Data out access time	tACC	CL = 30 pF	–	30	
Data out hold time 1	tOH1	–	10	–	
Data out hold time 2	tOH2	–	10	–	

*1: All timing is provided for based on 20% and 80% of VDD.
*2: rise time (tr) and fall time (tf) is defined max.10 ns.

11.3. Reset

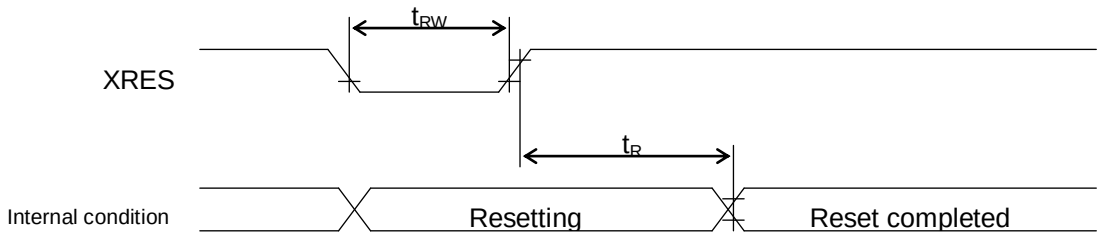


Fig 7 Reset

Table 15 reset characteristics

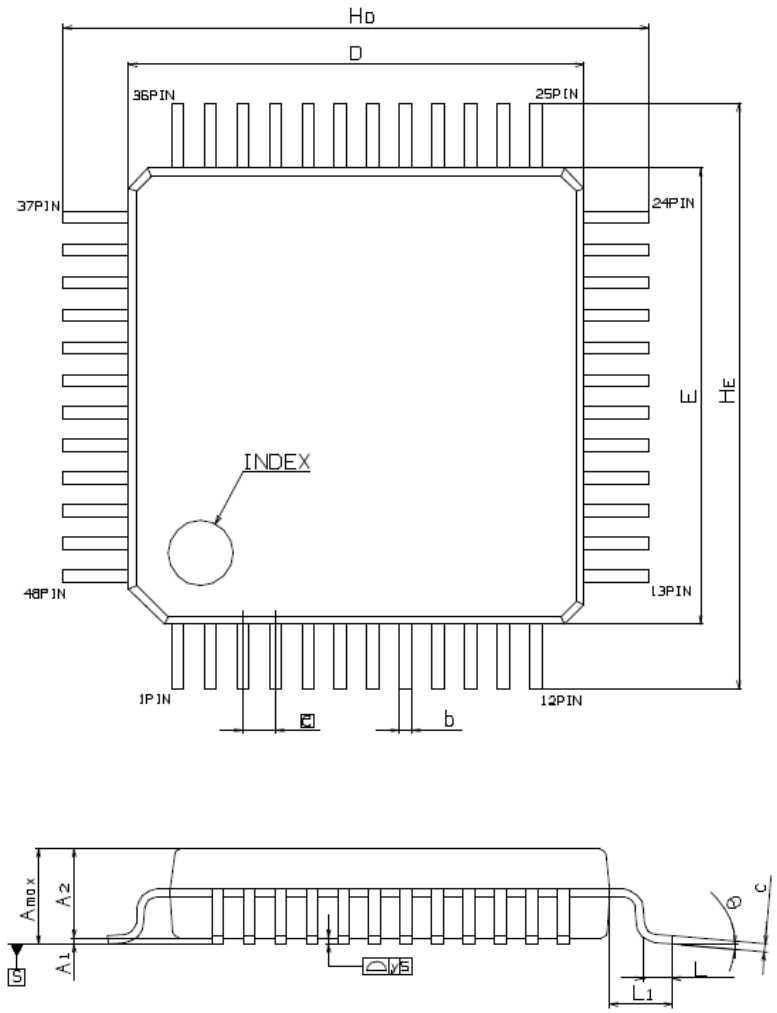
VSS = 0 V, VDDI = 1.65 to 3.6V, VDDL = 1.65 to 1.95V, VDD = 3.0 to 3.6 V, Ta = -40 to 85 ºC

item	code	conditions	Min.	Max.	unit
Reset time	tR	-	-	1	µs
Reset low level pulse width	tRW	-	20	-	

*1: All timing is provided for based on 20% and 80% of VDD.
*2: rise time (tr) and fall time (tf) is defined max.10 ns.
*3: When the power supply is turned on, the terminal XRES is recommended to be fixed at the “L" level.
*4: This condition is valid when resetting under stable power supply condition.

12. Package outer dimension

12.1.QFP12-48PIN

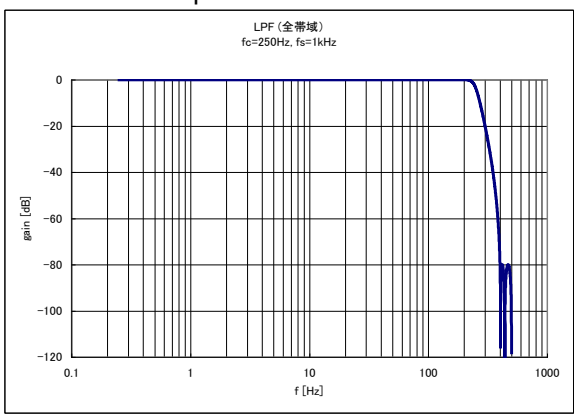


Symbol	Dimension in Millimters		
	Min	Nom	Max
E	-	7	-
D	-	7	-
A_{max}	-	-	1.7
A_1	-	0.1	-
A_2	-	1.4	-
e	-	0.5	-
b	0.13	-	0.27
c	0.09	-	0.2
θ	0°	-	10°
L	0.3	-	0.7
L_1	-	1	-
HE	-	9	-
HD	-	9	-
y	-	-	0.08

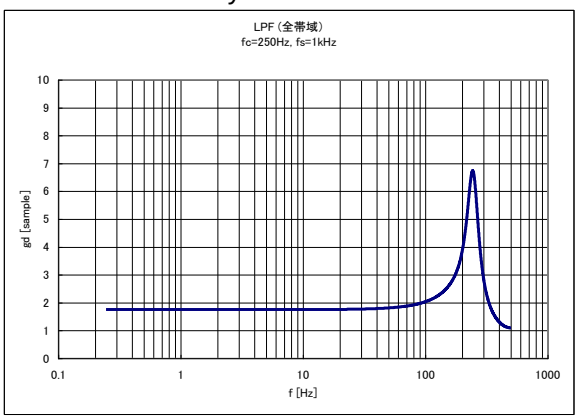
13. Digital filter characteristics

■Cut off frequency fc=250Hz, sampling frequency fs=1 kHz

Amplitude characteristic

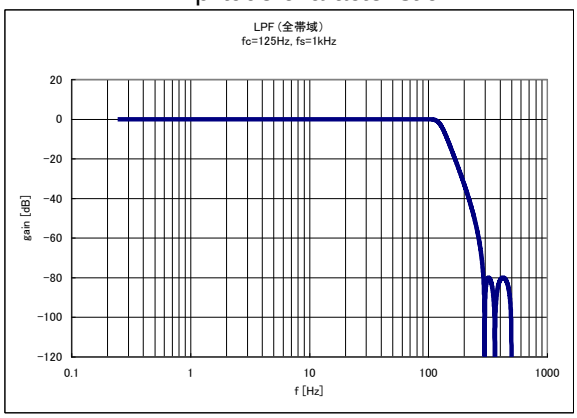


Delay characteristic

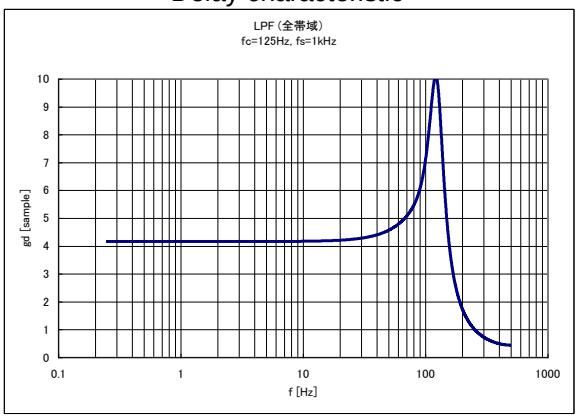


■Cut off frequency fc=125Hz, sampling frequency fs=1 kHz

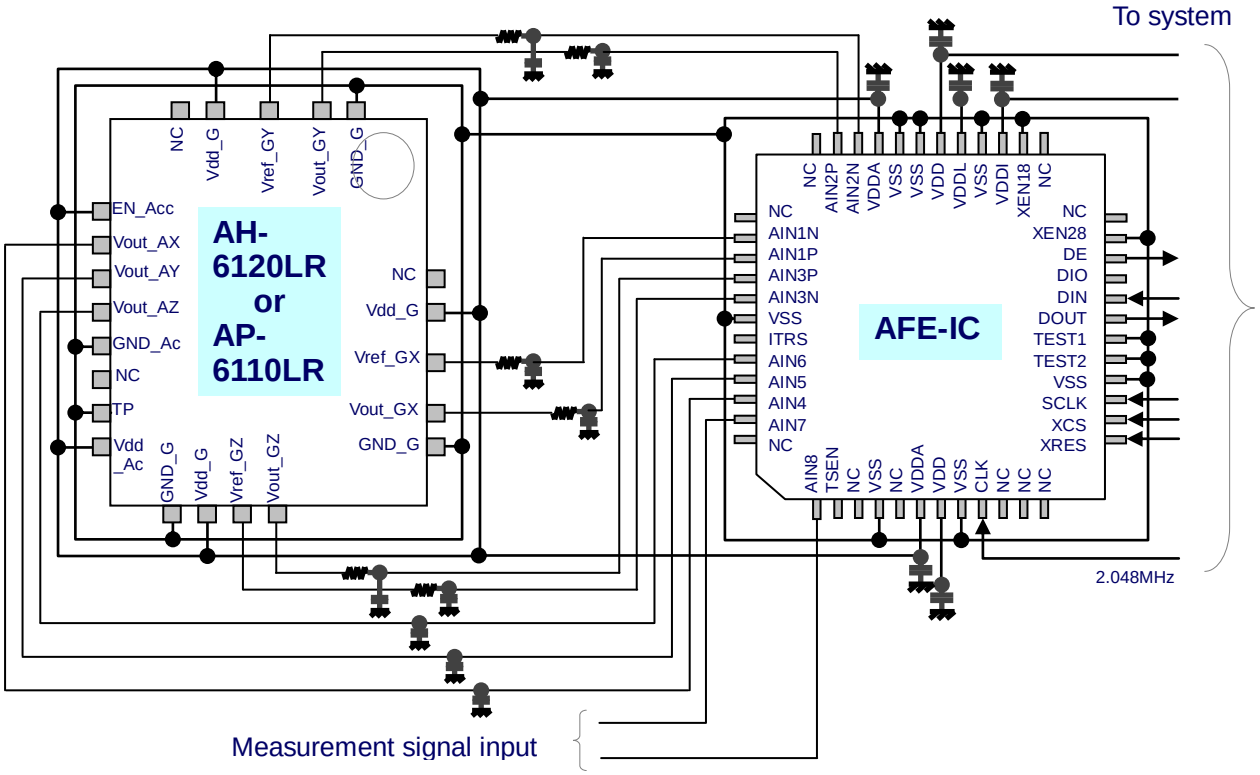
Amplitude characteristic



Delay characteristic



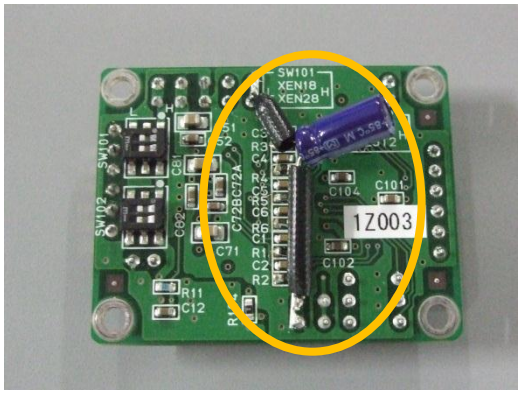
14. Wiring example



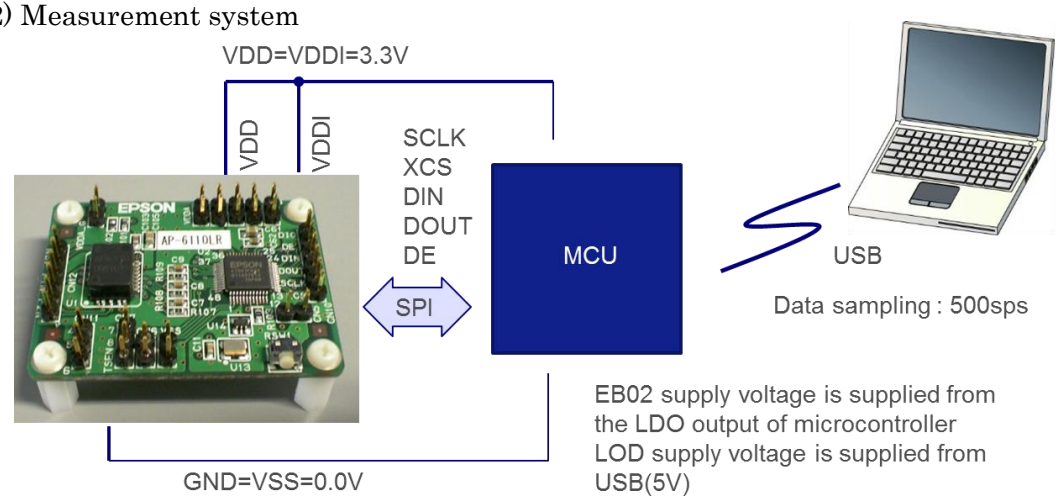
15. The method of output code stabilization

We introduce the contents of evaluation checked at our company to the stabilization method of output code.

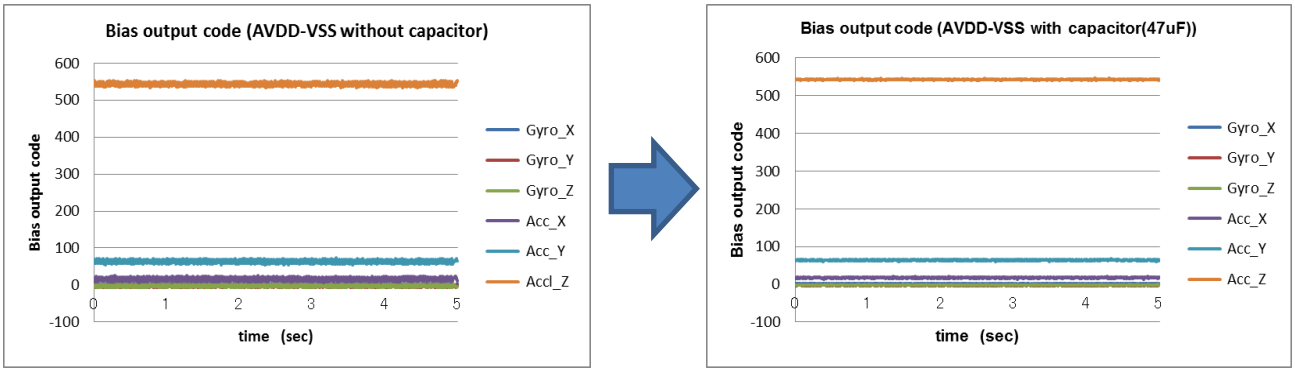
1) It adds 47uF between AVDD （CN3) and VSS(CN9-2)



2) Measurement system



3) Measurement results



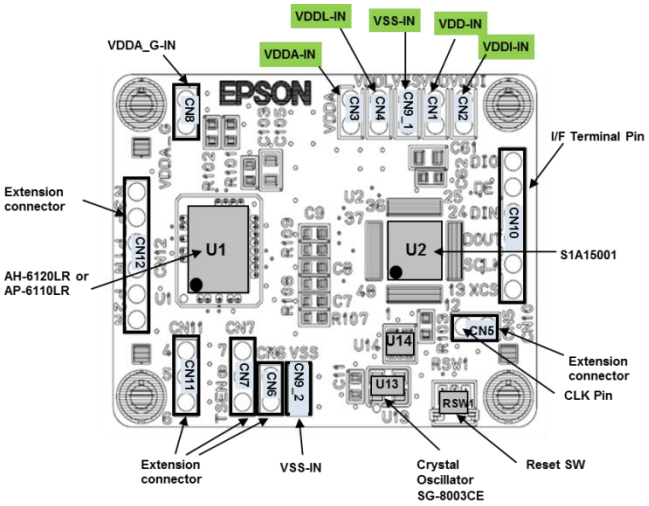
Standard deviation	Gx	Gy	Gz	Ax	Ay	Az
Without capacitor	2.413	2.398	2.357	4.187	4.150	4.562
With capacitor(47uF)	0.517	0.491	0.485	1.182	1.142	1.131

The code is stable by adding a capacitor between AVDD and VSS.

16.The method of analog output monitor

(1)How to monitor an analog output using a power supply with built-in AFE

The Gyro output can check CN12 pin and an acceleration output from CN11 pin, respectively.
When you don't remove R1-6 and R107-109 which constitute the passive filter connected to the sensor output, please take into consideration the influence of capacitance C1-9 (20nF).
If you would like to avoid the influence of the passive component part which constitutes the passive filter, please remove R1-6 and R107-109.



CN4(VDDL)
CN3(VDDA) — open
CN1(VDD) — 3.2V
CN2(VDDI)
CN9_1(VSS) — 0V

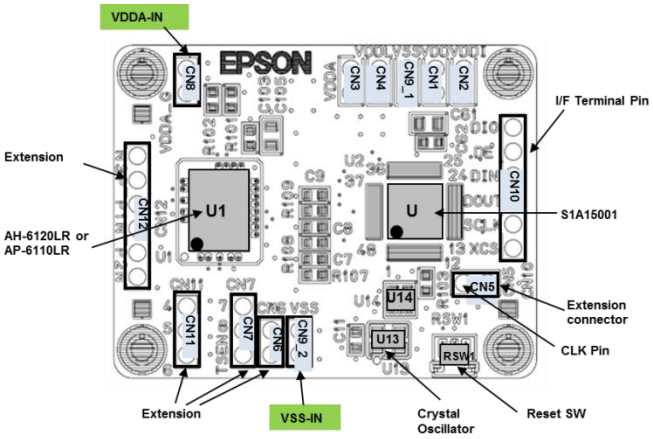
SW101 control
XEN18=L
XEN28=L
SW102 control
TEST1=L
TEST2=L

CN10(DIO) — open
(DE)
(DIN)
(DOUT)
(SCLK)
(XCS)
— Connected to system
(VDDA starting command issue)

(2)How to monitor an analog output using external power supply

The Gyro output can check CN12 pin and an acceleration output from CN11 pin, respectively.
When using an external power supply, it is necessary to change the parts on a substrate.
About the step to change the parts on a substrate.

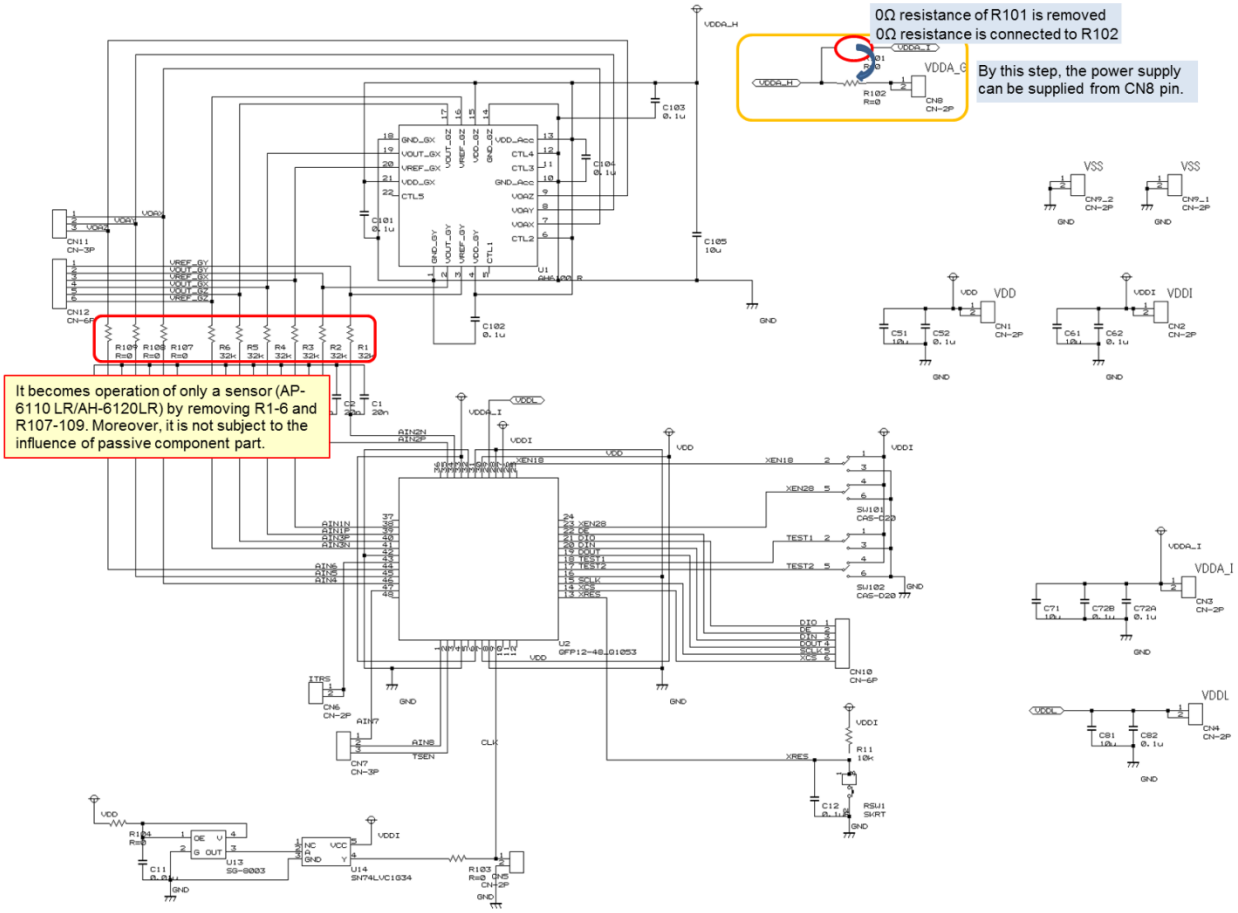
- The 0Ω resistance of R101 is removed, and 0Ω resistance is connected to R102.
  (By this step, the power supply can be supplied from CN8 pin.)
- When you avoid the influence of the passive component part which constitutes the passive filter connected to the sensor output, please remove resistance of R1-6 and R107-109.



CN8(VDDA) — 3V
CN4(VDDL)
CN3(VDDA)
CN1(VDD) — open
CN2(VDDI)
CN9_1,2(VSS) — 0V

SW101 Control
XEN18=L
XEN28=L
SW102 Control
TEST1=L
TEST2=L

CN10(DIO)
(DE)
(DIN)
(DOUT)
(SCLK)
(XCS)
— open


0Ω resistance of R101 is removed
0Ω resistance is connected to R102
By this step, the power supply can be supplied from CN8 pin.
It becomes operation of only a sensor (AP-6110 LR/AH-6120LR) by removing R1-6 and R107-109. Moreover, it is not subject to the influence of passive component part.

17.Contact

America

Epson Electronics America, Inc.
214 Devcon Drive, San Jose, CA 95112, USA
Phone: +1-800-228-3964 FAX: +1-408-922-0238

Europe

Epson Europe Electronics GmbH
Riesstrasse 15, 80992 Munich, GERMANY
Phone: +49-89-14005-0 FAX: +49-89-14005-110

Asia

Epson (China) Co., Ltd.
7F, Jinbao Bldg., No.89 Jinbao Street Dongcheng District, Beijing, China, 100005
Phone: +86-10-8522-1199 FAX: +86-10-8522-1120

Shanghai Branch
High-Tech Building, 900 Yishan Road, Shanghai 200233, China
Phone: +86-21-5423-5577 FAX: +86-21-5423-4677

Shenzhen Branch
12/F, Dawning Mansion, #12 Keji South Road, Hi-Tech Park, Shenzhen, China
Phone: +86-755-2699-3828 FAX: +86-755-2699-3838

Epson Hong Kong Ltd.
Unit 715-723 7/F, Trade Square, 681 Cheung Sha Wan Road, Kowloon, Hong Kong
Phone: +852-2585-4600 FAX: +852-2827-2152

Epson Taiwan Technology & Trading Ltd.
14F, No. 7, Song Ren Road, Taipei 110, TAIWAN
Phone: +886-2-8786-6688 FAX: +886-2-8786-6660

Epson Singapore Pte., Ltd.
No 1 HarbourFront Place, #03-02 HarbourFront Tower One, Singapore 098633
Phone: +65-6586-5500 FAX: +65-6271-3182

Seiko Epson Corp. Korea Office
5F (63Bldg.,Yoido-dong) 50, 63-ro, Yeongdeungpo-gu, Seoul, 150-763, Korea
Phone: +82-2-784-6027 FAX: +82-2-767-3677